Application Note

Biasing GaN and LDMOS RF Power Amplifiers in Aerospace Applications Using AFE11612-SEP

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ABSTRACT

This application note details the basic functions and benefits of the AFE11612-SEP in voltage biasing for radio frequency power amplifiers in space-rated applications. This report reviews the fundamentals of power amplifier biasing and supporting circuitry.

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Trademarks

1 LDMOS and GaN Power Amplifier FET PA Basics

Most radio frequency (RF) antenna systems feature power amplifiers (PA) for their RF transmitter design. Many aerospace and space applications include antenna systems, such as:

- Radar
- Radar Imaging Payload
- Communications Payload
- Telemetry

PA biasing circuits are implemented in RF antenna systems to ensure two things. First, that the power output of the amplifier is known and controlled, and second, that the system is powered on and off safely to reduce the risk of damaging the PA. PAs are commonly designed with either gallium nitride (GaN) or laterally diffused MOSFET (LDMOS) transistors. Power output in both GaN and LDMOS FETs (field-effect transistors) is dependent on the current that flows through the device from the drain to the source (I_{DS}).

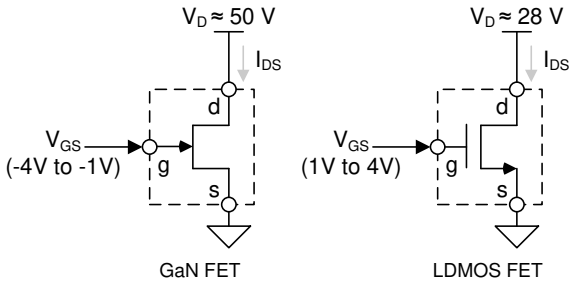


Figure 1-1. GaN and LDMOS FETs

I_{DS} is determined by a few variables: the drain voltage (V_D or V_{DRAIN}), the gate voltage (V_{GS}), and temperature. Figure 1-2 shows an example of I_{DS} values against the V_{DRAIN} for a selection of V_{GS} voltages for a GaN PA. The higher V_{GS} voltages result in a higher I_{DS}, or more power from the amplifier. When V_{GS} is sufficiently low, the PA allows virtually zero I_{DS} current. This V_{GS} voltage is called the *pinch-off* voltage. I_{DS} is also dependent on the V_{DRAIN}, but most designers do not vary the V_D. Instead, designers use optimized V_{DRAIN} voltages for the desired power levels. The V_{DRAIN} values are usually about 50 V for GaN PAs and 28 V for LDMOS PAs.

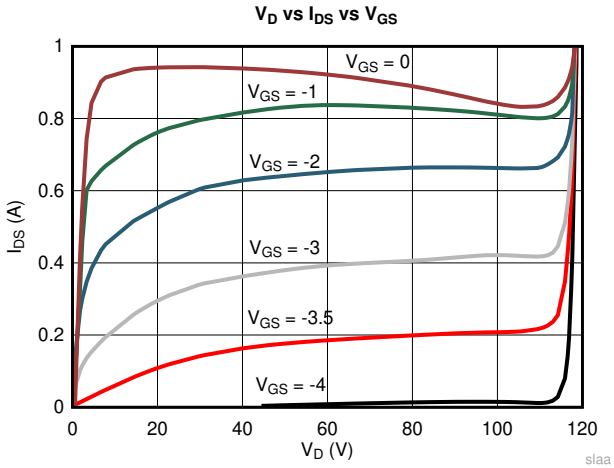


Figure 1-2. FET V_D, I_{DS}, and V_{GS} Behavior

2 V_{GS} Compensation

I_{DS} is dependent on the temperature of the PA. The I_{DS} variations due to thermal drift create the need to compensate the PA by adjusting one of the other two variables in the system: V_{DRAIN} or V_{GS}. Although there are many reasons why adjusting V_{DRAIN} is implemented in different RF applications, the response of the output power is minimal compared to the change in the V_{DRAIN} voltage, as shown in Figure 1-2. Adjusting V_{GS} allows for faster response time and total amplitude of the output power making it more practical for temperature compensation and other applications.

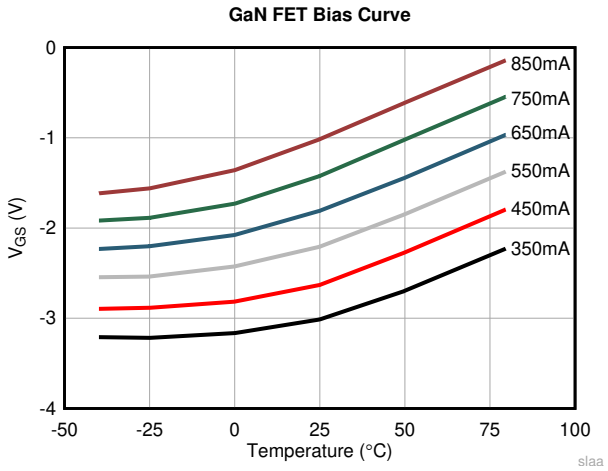


Figure 2-1. GaN PA V_{GS} Bias Voltage vs Temperature to maintain constant I_{DS}

Figure 2-1 shows V_{GS} needs to be adjusted to ensure a static I_{DS} due to thermal drift. Applications utilizing these PAs require implementing this kind of compensation to ensure that the power of the antenna system is tightly controlled. V_{GS} compensation can be implemented by either measuring the temperature of the PA, or measuring the I_{DS} using a current shunt and adjusting the V_{GS} accordingly.

3 Sequencing

Powering the PA on and off in a controlled routine is necessary to prevent the V_{GS} voltage from being too high when the V_{DRAIN} is applied. Such a state causes the PA to operate in saturation mode which may result in thermal damage in the PA or the board it is mounted on. Powering on a PA requires the following steps:

1. First, apply the V_{GS} signal to the PA. The V_{GS} voltage must transition to the V_{GS} pinch-off voltage or lower. This ensures that when the V_{DRAIN} voltage is applied, the gate is already low.
2. Next, enable the drain voltage supply and allow the V_{DRAIN} to be powered to the nominal value (50 V, for example). As the V_{GS} is at the pinch-off voltage, I_{DS} must be minimal.
3. After the V_{DRAIN} is applied, increase the V_{GS} bias voltage to set the desired power output of the PA.
4. Finally, enable the RF signal. This allows the PA to transmit a signal.

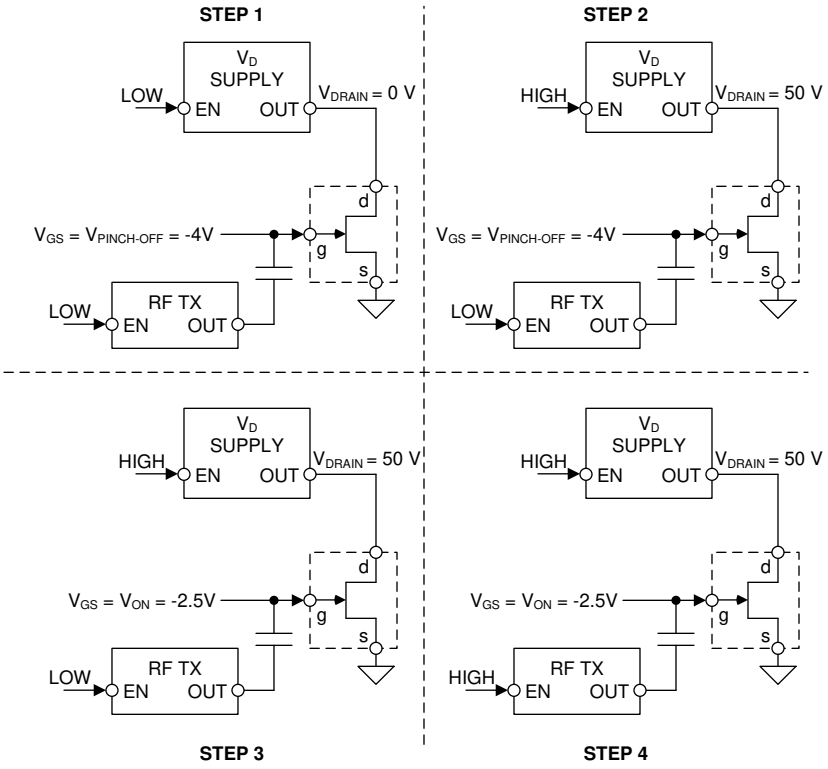


Figure 3-1. GaN Power Sequencing

The PA can be safely shut down by reversing the power-on steps.

1. Disable the RF signal from the PA.
2. Reduce the V_{GS} voltage to the pinch-off value, eliminating the power output of the PA.
3. Disable the V_{DRAIN} voltage by sending a disable signal to the drain supply.
4. Finally, the V_{GS} voltage can be allowed to collapse to ground as the PA is fully disabled.

4 An Integrated PA Biasing Solution

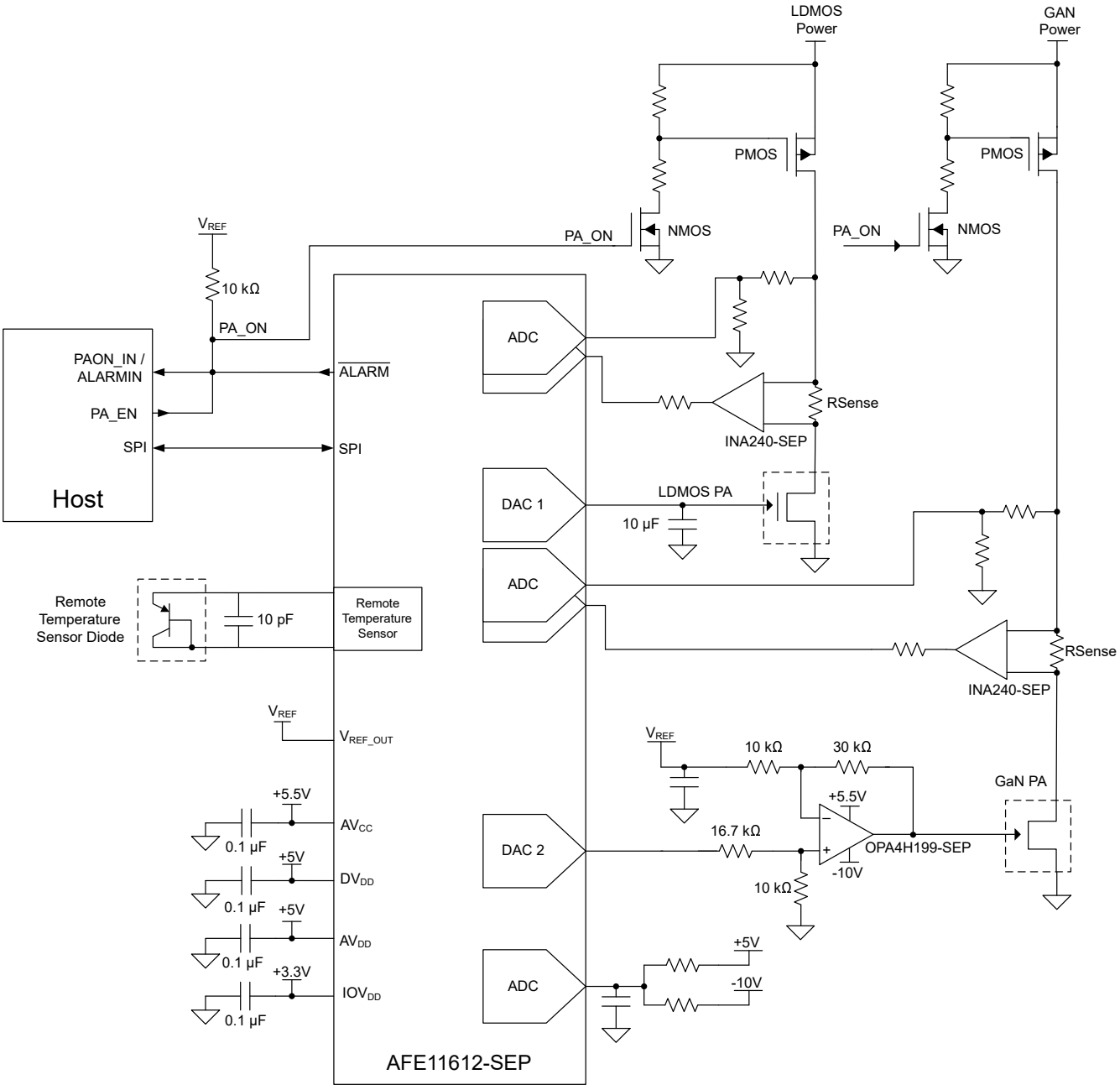


Figure 4-1. AFE11612-SEP Typical Application

The AFE11612-SEP is an integrated power-amplifier biasing solution that features precision Digital-to-Analog Converters (DACs) to allow for V_{GS} control of up to twelve LDMOS PAs and supports GaN PAs with additional circuitry. The device also features robust PA monitoring and protection with programmable thresholds for two remote temperature sensors and four out of the sixteen Analog-to-Digital Converter (ADC) inputs.

Additional devices used in the application are an operational amplifier with a 40 V bipolar supply range (OPA4H199-SEP), and a current-sense instrumentation amplifier with a common mode voltage range of -4 V to 80 V (INA240-SEP).

5 Negative GaN Biasing

The AFE11612-SEP features twelve 12-bit DACs. The device has an internal 2.5-V reference that scales the DAC output range from 0 V to 5 V. GaN PAs require negative gate voltage to be properly biased, with pinch-off voltages being more negative than the on voltages. The DAC output can be converted to a negative voltage through the use of a differential op-amp circuit that is powered by a negative power supply (V_{SS}). The following circuit uses the op-amp OPA4H199-SEP to offset and scale the 5-V output range to -7.5 V to 0 V. A differential op-amp circuit is used to protect the PA in case of an alarm shutdown. In an alarm state, the DAC drives the voltage to 0 V. The differential circuit outputs -7.5V to the GaN gate, thus ensuring the GaN PA turns off. The use of an inverting amplifier configuration is not recommended as the *off state* drives the output to 0 V, which can damage the PA in an alarm state.

The AFE11612-SEP 2.5 V reference output provides the offset voltage for the differential circuit. The resistors in the circuit were selected with the purpose of providing a -7.5 V to 0 V output range, while not significantly loading V_{REF}. The OPA4H199-SEP has a 40-V supply range, and the circuit can be modified to support greater negative-voltage applications if needed.

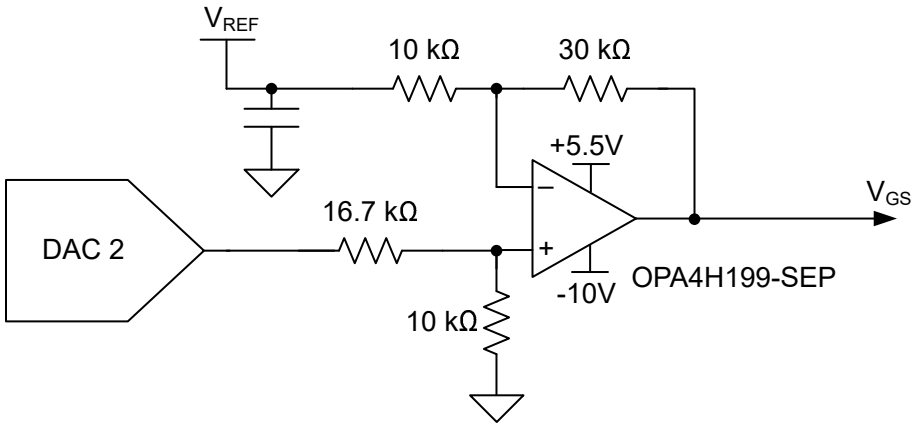


Figure 5-1. Differential Operational Amplifier Circuit

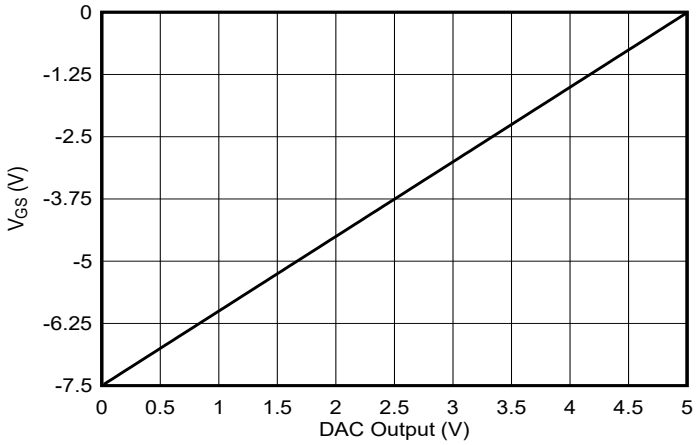


Figure 5-2. Differential Operational Amplifier Output

6 V_{DRAIN} Switching Circuit

The V_{DRAIN} protection circuit uses NMOS and PMOS transistors to disable the voltage being applied to the PA drain. This PA_ON circuit functions as a high-voltage switch. The V_{DRAIN} should be disabled at key times during startup, shutdown, and alarm events. This is achieved in this design by this NMOS and PMOS circuit. When the PA_ON voltage, described in the next section, is applied to the NMOS gate, the circuit turns on to allow V_{DRAIN} through the PMOS. Picking an NMOS with a V_{GS} voltage lower than 2.5 V is ideal, as the PA_ON circuit uses the AFE11612-SEP external 2.5-V reference as its digital output voltage level.

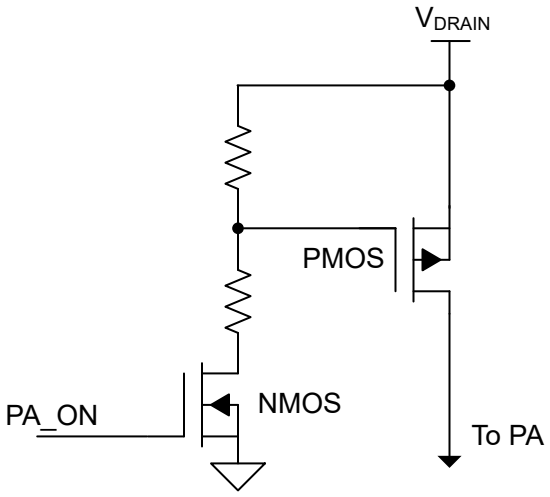


Figure 6-1. V_{DRAIN} Enable Circuit

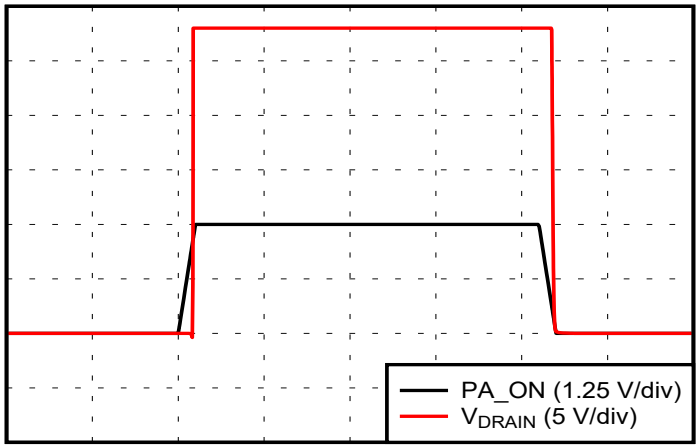


Figure 6-2. V_{DRAIN} Enable Plot

7 Controlled Gate Sequencing Circuit

It is important to control the PA during startup, shutdown, and alarm conditions, to ensure that the PA is not damaged during these events. The controlled gate-sequencing circuit uses open-drain signals to control the PA. An open-drain configuration is ideal in this case, as it allows the use of multiple digital and analog signals to be AND'd with each other to control the PA_ON signal. PA_ON asserts low during startup, shutdown, and alarm events, while allowing the host process to disable the drain. This is accomplished by effectively creating a three input logic AND gate of key signals: $V_{REF,}$ HOST PA_EN, and $\overline{ALARM}$.

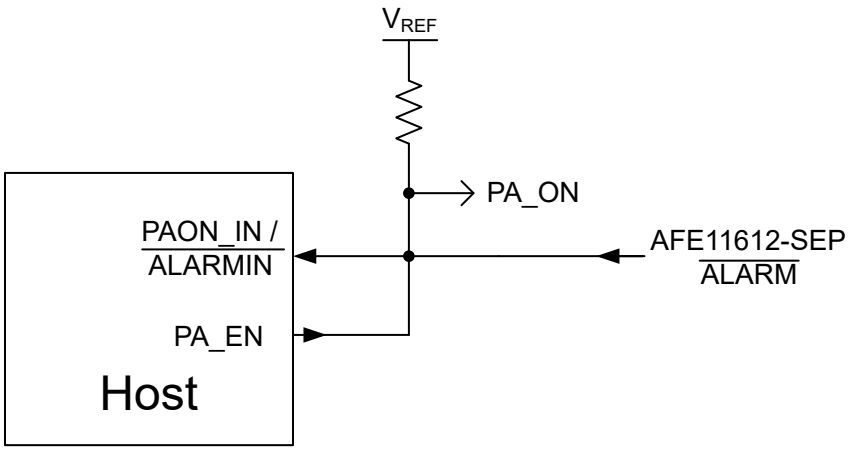


Figure 7-1. PA_ON Circuit

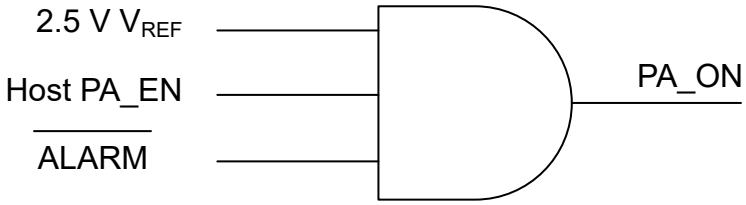


Figure 7-2. PA_ON Digital Logic Representation

V_{REF} is used as the voltage supply for the PA_ON. This ensures that the PA never has the drain voltage applied to it at startup, as the V_{REF} must be enabled by the host controller after the AFE11612-SEP starts up. Similarly, the PA does not have the drain voltage applied to it after the AFE1112-SEP turns off, as V_{REF} is shut down. The $\overline{ALARM}$ signal from the AFE11612-SEP is open-drain, which allows the circuit to force the PA_ON to 0 V if the AFE11612-SEP detects any alarms. Finally, the host microcontroller has the option of turning off PA_ON. The following truth table shows how all of the digital outputs interact with the PA_ON.

Table 7-1. PA_ON Truth Table

VREF	PA_EN	ALARM	PA_ON
0 V	X	X	0 V
2.5 V	Hi-Z	Hi-Z	2.5 V
2.5 V	L	Hi-Z	0 V
2.5 V	Hi-Z	L	0 V
2.5 V	L	L	0 V

The PA_ON is controlled at startup and shutdown by being pulled up to V_{REF}. The AFE11612-SEP internal 2.5-V reference voltage is not enabled at startup, so the initial 0 V output prevents the PA from being on at startup. The host then initializes the device, powers on the V_{REF}, and then controls the PA_ON with an PA_EN digital output from the host. Here is an example of the PA_ON power on sequence:

1. The AFE11612-SEP is initialized. This turns on the V_{REF}. With no alarm state at startup, the $\overline{ALARM}$ pin is High-Z. The host pulls PA_EN low to keep the PA off.

2. Next, the drain power is turned on. The host sets PA_EN to High-Z, setting the PA_ON to 2.5 V and turning on the PA.
3. Third, an alarm condition is shown. The $\overline{\text{ALARM}}$ goes to 0 V, turning off the PA_ON and thus turning off the PA to protect it.
4. Fourth, the alarm condition is cleared. $\overline{\text{ALARM}}$ returns to High-Z, and the PA_ON is on.
5. Lastly, before the part powers off, it is safe to turn off the PA_ON via the host controller, then power down the AFE11612-SEP.

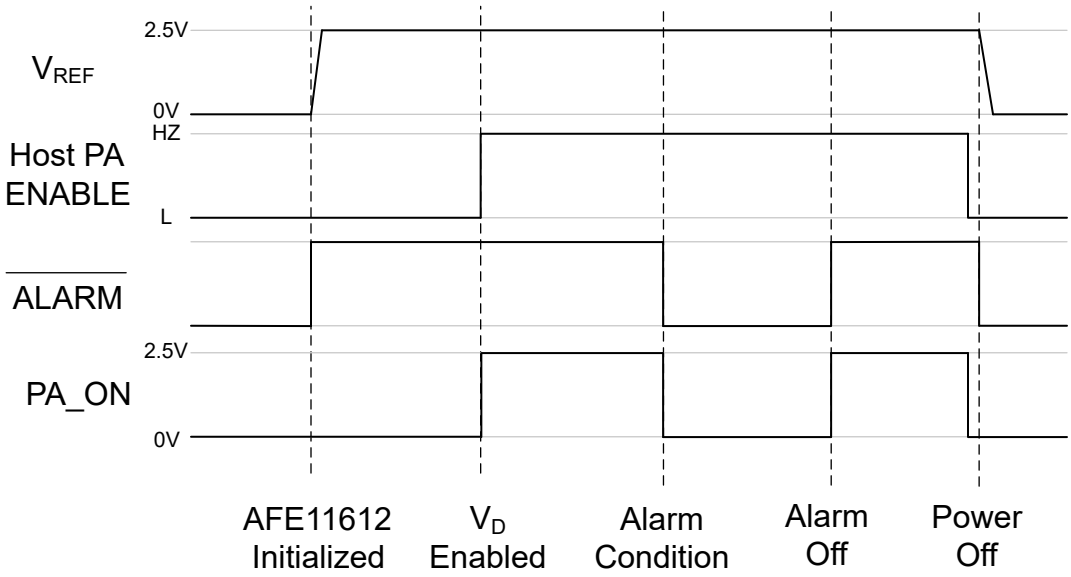


Figure 7-3. PA_ON Power Sequence Control

8 V_{DRAIN} Monitoring

It is important to monitor the V_{DRAIN} voltage to ensure the PA Drain supply is operating at the expected voltage. A resistor divider is required to properly scale the V_{DRAIN} voltage, as the voltage range for the ADC is selected to be 0 V to 2.5 V or 0 V to 5 V. This can be accomplished using the integrated successive-approximation register (SAR) ADC in the AFE11612-SEP. SAR ADCs have an internal sampling capacitor which must be charged every time there is an ADC conversion. This capacitor must be charged within the sample acquisition time to ensure the ADC measures the voltage correctly. This is done using a charge-bucket filter with an external capacitor (C_{FILT}) of approximately 1nF. The impedance of the resistor divider must be limited, ideally under 10 kΩ to allow sufficient current to charge the sampling capacitor.

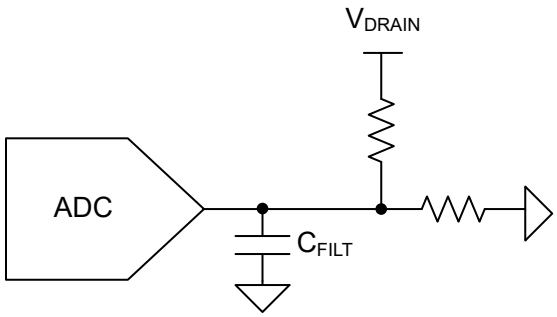


Figure 8-1. V_{DRAIN} Monitor Circuit

9 I_{DQ} Monitoring

Monitoring the drain quiescent current (I_{DQ}) can detect if the PA is efficiently conducting the desired current. An external INA can be used to convert current measurements into voltage outputs for the AFE11612-SEP. The INA used in this example circuit is the INA240-SEP, which features a 20 V/V gain. With the following equation, the ideal voltage differential across the resistor is calculated, where V_{DIFF} is the maximum differential-input voltage across the INA's inputs, V_{OUT} is the ADC range of 2.5 V or 5 V, and gain is 20 V/V. This calculation gives a maximum voltage differential of 125 mV for 2.5-V ADC range or 250 mV for 5-V ADC range across the resistor.

$V_{DIFF} = V_{OUT} / GAIN$

Next, use the following equation to calculate resistance. R_{SENSE} is the shunt resistor value; V_{DIFF} is the previously calculated maximum voltage drop of 125 mV or 250 mV; and I_{DQ_MAX} is the maximum current draw of the power amplifier.

$R_{SENSE} = V_{DIFF} / I_{DQ\_MAX}$

Similar to the V_{DRAIN} monitoring circuit, an external RC filter is required for current charging.

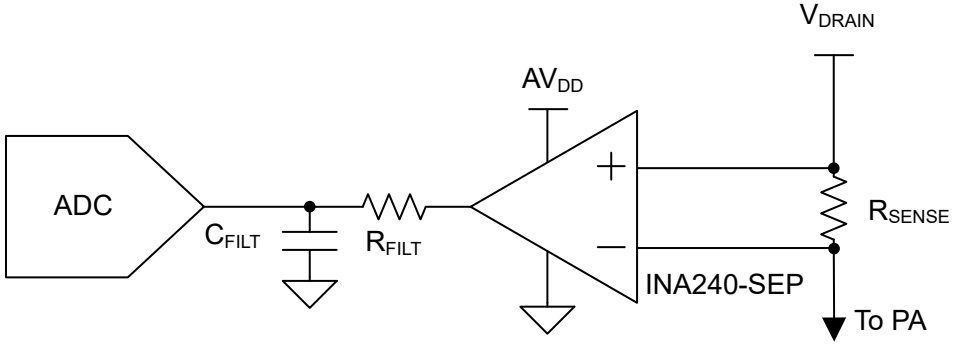


Figure 9-1. I_{DQ} Monitor Circuit

10 External Negative Power Supply Monitoring

GaN PAs can be damaged if the V_{GS} potential increases to too high, resulting in PA saturation. If the V_{SS} supply collapses (meaning it slews to 0 V), this condition can occur as the differential op-amp circuit requires a negative supply. Thus, it is critical to monitor the V_{SS} supply for collapse events. Monitoring can be done using a simple resistor divider biased by an external reference voltage, such as 5 V used for the device analog supply, to scale the negative V_{SS} supply voltage to the ADC input range. If the external 5-V supply were to collapse, this would shut down the AFE11612-SEP and therefore shut down the PA_ON circuit. A zener diode can be added for additional protection in case of the external 5-V supply collapsing.

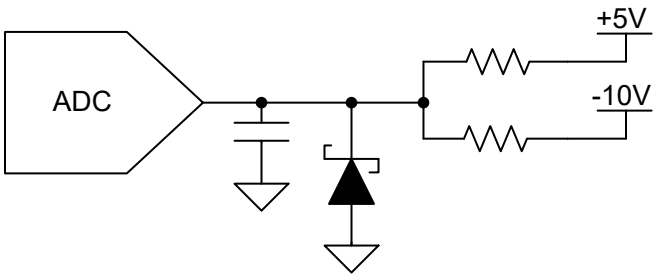
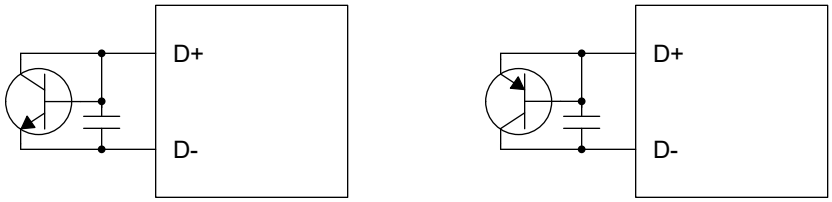


Figure 10-1. V_{SS} Monitor Circuit

11 PA Temperature Monitoring

The AFE11612-SEP has two sets of remote temperature sensor inputs that can be used to monitor the temperature of two diode-connected transistors placed near the PAs. The two temperature sensors have programmable alarm thresholds that can trigger an alarm state and disable the PA_ON.



(a) NPN (b) PNP

Figure 11-1. Remote Temperature Circuit

12 Summary

Power amplifier behavioral nuances make discrete V_{GS} compensation solutions complex and costly. The AFE11612-SEP simplifies the solution while adding beneficial features, such as gate monitoring, V_{DRAIN} monitoring, temperature monitoring, and supply collapse detection for startup and shutdown sequence control, to make the device an excellent value.

Table 12-1. Device Recommendations

Device	Optimized Parameters	Total Ionizing Dose (TID) Characterized	Single Event Latch-Up (SEL) Characterized
AFE11612-SEP	Space enhanced 12 12-bit DACs with 16 12-bit ADC inputs.	20 krad(SI)	Immune to 43 MeV-cm^2/mg at 125°C
OPA4H199-SEP	Space enhanced high voltage quad-output operational amplifier.	30 krad(SI)	Immune to 43 MeV-cm2 /mg at 125°C
INA240-SEP	Space enhanced wide common-mode range current sense amplifier.	20 krad(SI)	Immune to 43 MeV-cm2 /mg at 125°C

13 References

- Texas Instruments, *AFE11612-SEP Radiation-Tolerant, Analog Monitor and Controller With Multichannel ADC, DACs, and Temperature Sensors*, data sheet.
- Texas Instruments, *OPA4H199-SEP 40-V, Radiation Hardened, Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Op Amp in Space Enhanced Plastic*
- Texas Instruments, *INA240-SEP Wide Common-Mode Range, High- and Low-Side, Bidirectional, Zero-Drift, Current-Sense Amplifier in Space Enhanced Plastic*
- Texas Instruments, *Temperature Compensation of Power Amplifier FET Bias Voltages*, application note.

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