

ADS52J90 8/16/32-Channel, Analog-to-Digital Converter Evaluation Module

This user's guide gives an overview of the evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS52J90 analog-to-digital converters (ADC). The ADS52J90 EVM provides a platform for evaluating the ADC under various signal, clock, reference, and ADC output formats. In addition, the EVM supports the testing of both an LVDS interface as well as a JESD204B interface.

NOTE: A different capture card EVM is required for each interface.

NOTE: In compliance with the Article 33 provision of the EU REACH regulation, we are notifying you that this EVM includes component(s) that contain at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are listed in [Table 1](#):

Table 1. List of SVHCs

Component Manufacturer	Component Part Number	SVHC Substance	SVHC CAS (When Available)
Abracan ABM8G	ABM8G	Diboron trioxide	1303-86-2
Abracan ABM8G	ABM8G	Lead oxide	1317-36-8

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Trademarks

1 Quick Views of Evaluation Setups for LVDS and JESD204B Interfaces

The ADS52J90 EVM can be tested using an LVDS data interface or a JESD204B data interface.

1.1 LVDS Interface (ADS52J90 EVM + TSW1400)

As shown in [Figure 1](#), mating the ADS52J90 EVM with a TSW1400 EVM allows testing using an LVDS data interface.

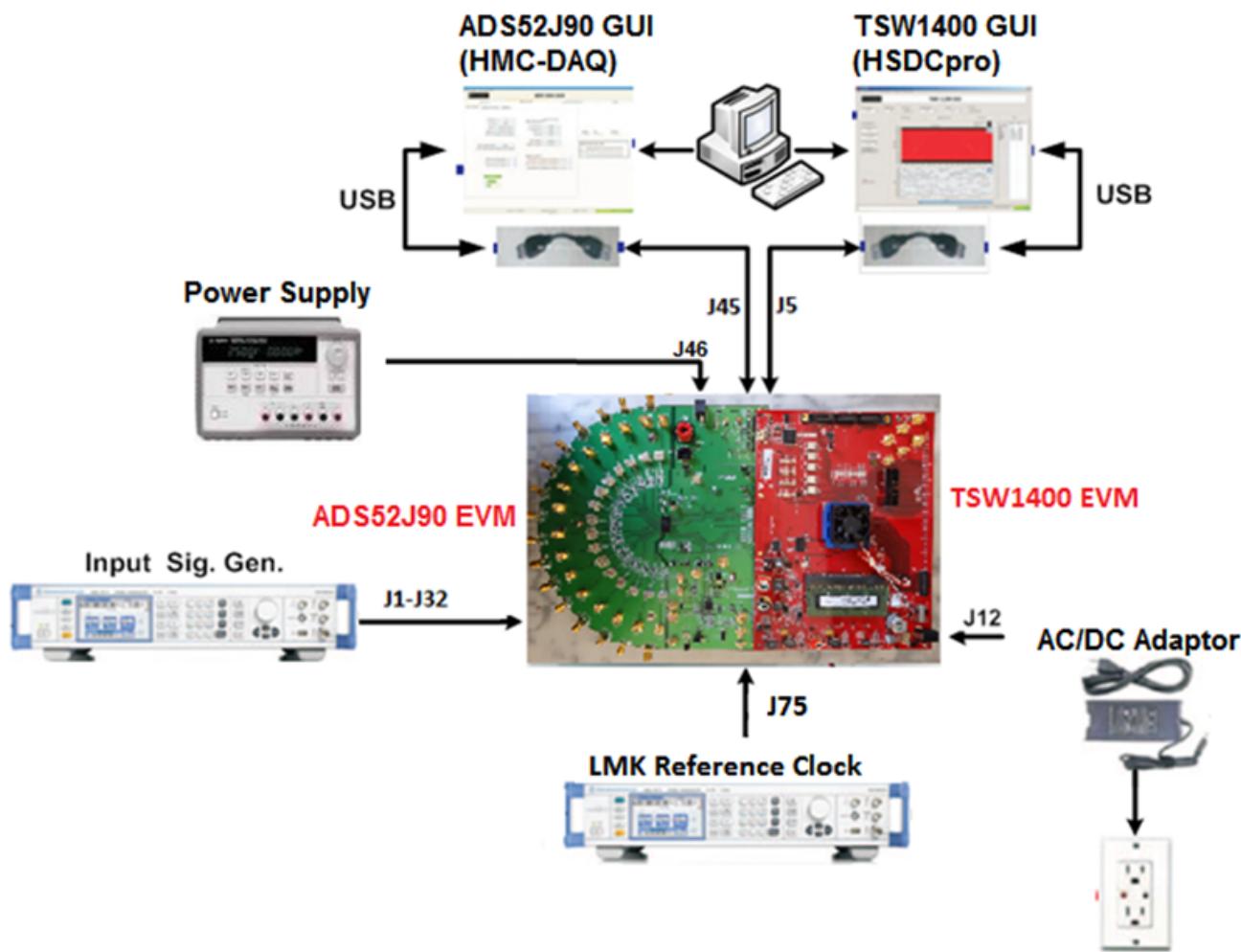


Figure 1. LVDS Evaluation Setup

FPGA EVM: The TSW1400 high-speed LVDS de-serializer EVM is required for capturing data from the ADS52J90EVM. Analysis of the captured data is possible using its graphical user interface (GUI) which is called High Speed Data Converter Pro.

NOTE: The same GUI is used to control the TSW14J56 capture card for supporting a JESD204B data interface.

For more information pertaining to be TSW1400EVM, see:
<http://focus.ti.com/docs/tools/folders/print/tsw1400evm.html>.

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, a band-pass filter (BPF) is required on the analog input signal to attenuate the harmonics and noise from the generators.

Power Supply: A single +5-V supply powers the ADS52J90EVM through connectors located at **J47** and **J48** or through an AC adaptor (not provided) at **J46**. The supply for the ADS52J90 device is derived from this +5-V supply. The power supply must be able to source up to 1.5 A. The TSW1400 EVM is powered through an AC adaptor provided with its EVM kit.

USB Interface to PC: The USB connections from the ADS52J90EVM and TSW1400EVM to the computer are used for communication from the GUIs to the boards. [Section 2](#) explains the *High Speed Data Converter Pro* and ADS52J90 GUI installation procedures.

1.2 JESD204B Interface (ADS52J90 EVM + TSW14J56)

As shown in [Figure 2](#), mating the ADS52J90 EVM with a TSW14J56 EVM allows testing using a JESD204B data interface.

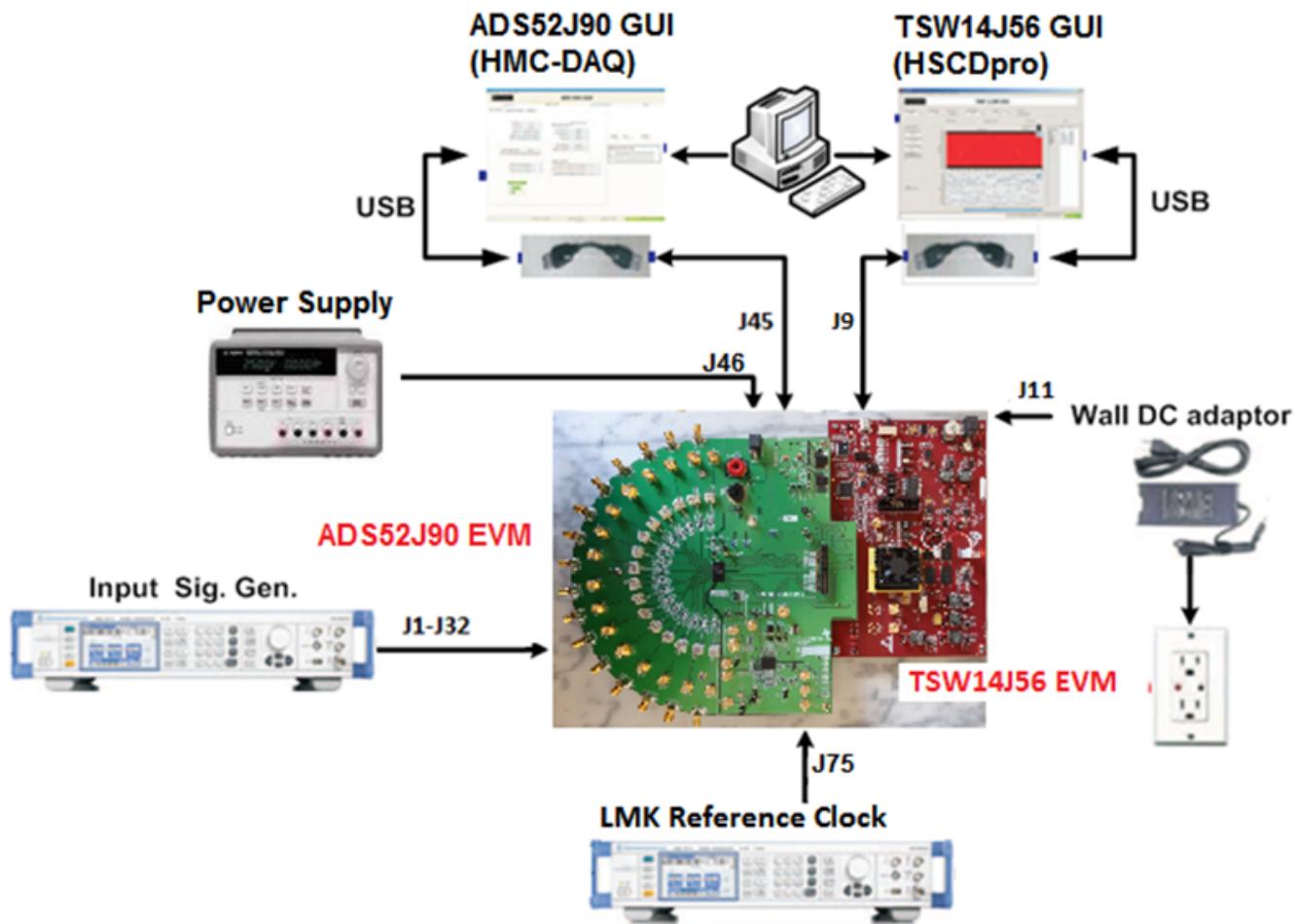


Figure 2. JESD204B Evaluation Setup

FPGA EVM: The TSW14J56 high-speed JESD204B de-serializer board is required for capturing data from the ADS52J90EVM. Analysis of the captured data is possible using its graphical user interface (GUI) which is called High Speed Data Converter Pro (*note: the same GUI is used to control the TSW1400 capture card for supporting an LVDS data interface*).

For more information pertaining to the TSW14J56EVM, see: <http://www.ti.com/tool/tsw14j56evm>

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, a band-pass filter (BPF) is required on the analog input signal to attenuate the harmonics and noise from the generator.

Power Supply: A single +5-V supply powers the ADS52J90EVM through connectors located at **J47** and **J48** or through an AC adaptor (not provided) at **J46**. The supply for the ADS52J90 device is derived from this +5-V supply. The power supply must be able to source up to 1.5 A. The TSW14J56 EVM is powered through an AC adaptor provided with its EVM kit.

USB Interface to PC: The USB connections from the ADS52J90EVM and TSW14J56EVM to the computer are used for communication from the GUIs to the boards. [Section 2](#) explains the *High Speed Data Converter Pro* and ADS52J90 GUI installation procedures.

2 GUI Software Installation

The ADS52J90 EVM and the de-serializing capture card EVM both require software installations. The following two sections explain where to find and how to install the software properly. Ensure that no USB connections are made to the EVMs until after the installations are complete.

2.1 High Speed Data Converter Pro (HSDCpro) GUI Installation

Download the [High Speed Data Converter Pro GUI Installer \(SLWC107\)](#) from the Texas Instruments website (www.ti.com) and install per the instructions in its user's guide ([SLWU087](#)).

NOTE: Version 3.1 or higher of HSDC Pro is required to test the ADS52J0. If an earlier version of HSDC Pro is installed, please uninstall before installing the latest version.

TI recommends installing HSDC Pro before installing the ADS52J90 GUI and installing it in the default location provided during installation.

2.2 ADS52J90 GUI Installation (HMC-DAQ)

The GUI used to control the ADS52J90 EVM is a suite that supports a family of devices. The GUI is called *Healthtech Multi-Channel Data Acquisition GUI*, or, *HMC-DAQ*. Download and save the file *HMC-DAQ_GUI_INSTALLER_SLOC326.zip* to a temporary location on the local PC hard drive. Once saved, unzip the file and run the executable as administrator by right clicking on the file. Follow the instructions provided during installation. TI recommends installing after HSDCpro has been installed and in the default location provided during installation.

3 ADS52J90 EVM Headers/Test Points and Clock Configuration

This section describes the functions of the headers on the EVM. It also provides a list of test points on the EVM that are useful for debug and general-use purposes. Finally, several options for providing clocks to the EVM are described.

3.1 ADS52J90 EVM Header Configuration

The ADS52J90 EVM is flexible in its configurability through the use of 2- and 3-pin headers. [Table 2](#) describes the purpose of all headers on the EVM and the default positions. With this configuration, all required clocks for testing the LVDS or JESD204B interface are derived from a single reference clock provided to SMA J75 to the LMK04826 clocking device installed at designator **U2** on the EVM. The LMK04826 is configured for Clock Distribution Mode (CDM) with the provided scripts.

Table 2. ADS52J90 Default Header Configuration

Jumper Description	Jumper#	Jumper Name	Default Config	Circuit	Description
Power Supply	JP9	+3.3VCLK	Short pins 1-2	Clocks	Power supply XTAL1, XTAL2, OSC1, LMK04826
	JP10	IOVDD_+3.3V	Short pins 1-2	SPI BUFFERS	Power supply for SPI level shifters and isolators
	JP11	DVDD_+1.2V	Short pins 1-2	ADS52JD90	+1.2-V digital power supply for ADS52JD90
	JP12	AVDD_+1.8V	Short pins 1-2	ADS52JD90	+1.8-V analog power supply for ADS52JD90
	JP13	LVDD_+1.8V	Short pins 1-2	ADS52JD90	+1.8-V digital power supply for ADS52JD90
	JP15	DISABLE	DNI	Regulator	Not used
	JP16	5VIN	DNI	Regulator	Not used
ADS52J90 SYNC Options	JP33	n/a	Short pins 1-2	ADS52JD90 SYNC pin	Selects SYNC signal source to ADS52JD90: (1) Auxiliary signal determined by JP28 or (3) GUI via FTDI device
	JP28	n/a	Short pins 1-2	ADS52JD90 SYNC pin	Selects auxiliary SYNC signal source to ADS52JD90: (1) SMA J50 or (3) FPGA via pin 105 of connector J44B
LMK04826 Options	JP2	SYNC	Short pins 1-2	LMK SYNC	Selects the source of SYNC signal into LMK042x clock device: (1) signal from SMA J39, LMK_SYNC or (3) signal from FPGA at pin K22 of connector J43C
	JP3	LMK_RB	Short pins 2-3	LMK Readback/Reset	Selects LMK RESET pin signal source: (1) LMK_DATA_OUT out to FTDI (3) LMK_RESET in from FTDI
ADC_CLKP/M SEL	JP39	ADC_CLK_AUX	Short pins 1-2	ADS52J90 CLKP/M & SYSREFP/M Source	Selects auxiliary CLKP/M signal source to ADS52JD90: (1) SMA J55, ADC_CLK or (3) one of two on-board XTAL oscillators determined by JP8
	JP40	ADC_CLK	Short pins 2-3		Selects signal source to CLKP/M of ADS52J90: (1) Auxiliary source from JP39 or (3) LMK04826 output
	JP41	ADC_SYSREF	Short pins 1-2		Selects signal source to CLKP/M of ADS52J90: (1) Auxiliary source from JP39 or (3) LMK04826 output
XTAL Power Supply Options	JP4	OSC1_VDD	Open	XTAL/OSC Power	Powers 100-MHz OSC1
	JP5	XTAL1_VDD	Open		Powers 10-MHz XTAL1
	JP6	XTAL2_VDD	Open		Powers 40-MHz XTAL2
XTAL SEL	JP7	LMK_CLKIN1	Short pins 1-2	LMK CLKIN1	Selects signal source to CLKIN1 of LMK04826: (1) SMA J75, LMK_CLKIN1 or (3) XTAL determined by JP8
	JP8	XTAL_SEL	Open	XTAL Oscillators	Selects XTAL source to JP7 and JP39: (1) 10MHz XTAL1 or (3) 40MHz XTAL2
Analog Inputs 8ch mode	JP700_7	n/a	Short pins 2-3	Analog Inputs 8ch mode	Selects between (1) 5-V power supply and (2) GND for amplifier on channels 7,8 for 8ch mode
	JP800_8	n/a	Short pins 2-3		

Jumpers **JP11**, **JP12**, **JP13** can be removed and individual power supplies given to these headers in order to monitor the DC current consumed by the ADS52J90.

3.2 ADS52J90 EVM Test points

[Table 3](#) lists all test points on the ADS52J90 EVM and their purposes.

Table 3. ADS52J90 EVM Test Points

Test Point	Silkscreen	Circuit	Description
TP13	+5.0V_IN	Power supply	Main +5-V power supply to EVM
TP15	GND	Power supply	Ground reference for EVM
TP14	IOVDD3.3V	Power supply	Power supply for VCM generation
TP12	+3.3VCLK	Power supply	Power supply for LMK0482x and oscillators
TP16	4V	Power supply	Input supply to regulator at designator U11
TP17	AVDD_+1.8V	Power supply	Power supply to ADS52J90
TP18	LVDD_+1.8V	Power supply	Power supply to ADS52J90
TP19	FORCE_VCM	Analog inputs	Can provide external VCM to analog inputs by installing R108 and uninstalling R110
TP20	FORCE_VREF	Analog inputs	Can provide external VREF to ADS52J90 by installing R109
TP1	VCM	Analog inputs	ADS52J90 output providing VCM to analog inputs
TP4	GTX_CLKP	LMK0428x output	GTX clock to FPGA on capture card
TP5	GTX_CLKM	LMK0428x output	GTX clock to FPGA on capture card
TP21	CLK_LA0_0P	LMK0428x output	Global clock to FPGA on capture card (typ. equals Fs)
TP22	CLK_LA0_0M	LMK0428x output	Global clock to FPGA on capture card (typ. equals Fs)
TP6	SYSREF_P	LMK0428x output	SYSREF clock to FPGA on capture card
TP7	SYSREF_M	LMK0428x output	SYSREF clock to FPGA on capture card
TP8	CLKP	LMK0428x output	Device clock (Fs) to DUT from LMK0482x
TP10	CLKM	LMK0428x output	Device clock (Fs) to DUT from LMK0482x
TP9	SYSREFP	LMK0428x output	SYSREF clock to DUT from LMK0482x
TP11	SYSREFM	LMK0428x output	SYSREF clock to DUT from LMK0482x
TP37	CLK_P	DET LAT EVM	Device clock (Fs) to DUT when Deterministic Latency EVM is used
TP38	CLK_M	DET LAT EVM	Device clock (Fs) to DUT when Deterministic Latency EVM is used
TP35	SYSREF_P	DET LAT EVM	SYSREF clock to DUT when Deterministic Latency EVM is used
TP36	SYSREF_M	DET LAT EVM	SYSREF clock to DUT when Deterministic Latency EVM is used
TP23	GND	GND	Ground reference for EVM
TP2	SYNCP_SERDES	JESD SYNC	Input JESD SYNC~ to ADS52J90 from FPGA
TP3	SYNCM_SERDES	JESD SYNC	Input JESD SYNC~ to ADS52J90 from FPGA
TPA0	SCLK	ADS52J90 SPI PIN	SPI clock input to ADS52J90
TPA1	SDATA	ADS52J90 SPI PIN	SPI data input to ADS52J90
TPA2	SEN	ADS52J90 SPI PIN	SPI enable input to ADS52J90
TPA3	SDOUT	ADS52J90 SPI PIN	SPI read back output from ADS52J90
TPA4	RESET	ADS52J90 PIN	RESET pin to ADS52J90
TPA5	PDN_GBL	ADS52J90 PIN	PDN_GBL pin of ADS52J90
TPA6	PDN_FAST	ADS52J90 PIN	PDN_FAST pin of ADS52J90
TPA7	SYNC_LVDS_FTDI	ADS52J90 PIN	SYNC pin to ADS52J90 allowing for synchronized LVDS outputs
TPB0	LMK_CLK	LMK SPI PIN	SPI clock input to LMK0482x
TPB1	LMK_DATA_OUT	LMK SPI PIN	SPI read back output from LMK0482x
TPB2	LMK_DATA	LMK SPI PIN	SPI data input to LMK0482x
TPB3	LMK_SPI_EN	LMK SPI PIN	SPI enable input to LMK0482x
TPB4	LMK_RESET	LMK PIN	RESET pin to LMK0482x
TPB5	RSV_DIG	n/a	Reserved
TP24	GND	GND	Ground Reference for EVM

3.3 EVM Clock Configuration

The EVM should be shipped with jumpers setting the LMK04826 clocking device (U2) in clock distribution mode. In this configuration shown in [Figure 3](#), the LMK04826 acts as a clock buffer/divider on the external input clock to SMA **J75, LMK_CLKIN1**. For LVDS mode, this input clock should be set to the desired system clock required by the ADS52J90. To support the JESD204B interface, this input clock should be set to 1/40 the SerDes line rate when the line rate is above 1Gbps and 1/10 the SerDes line rate when the line rate is below 1Gbps. Put another way, the SerDes lane rate will be 10x the reference clock when the calculated lane rate is below 1Gbps and will be 40x the reference clock when the calculated lane rate is above 1Gbps. The HSDCpro GUI will report both the calculated lane rate and the required reference clock each time the user changes the *Output Data Rate* value in the GUI. [Figure 4](#) and [Figure 5](#) show examples of the message when lane rate is 40x the reference clock and when the lane rate is 10x the reference clock, respectively. Configuration scripts for both 10x rate and 40x rate are provided in folders with the appropriate suffix appended to the folder names.

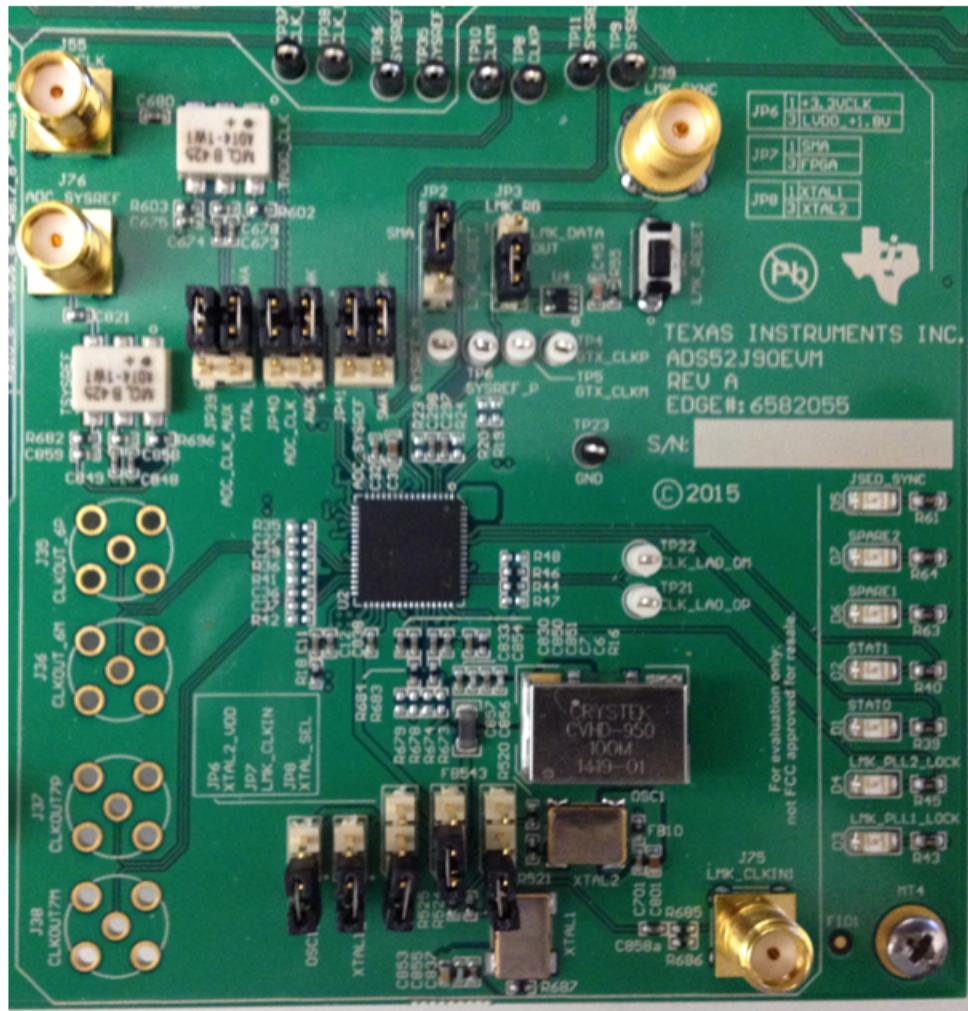


Figure 3. Clock Config: LMK CDM Mode

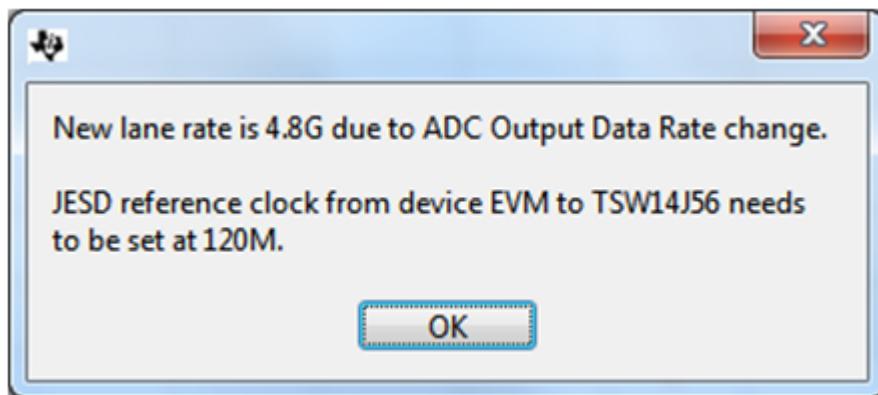


Figure 4. HSDCpro 40x Lane Rate Message

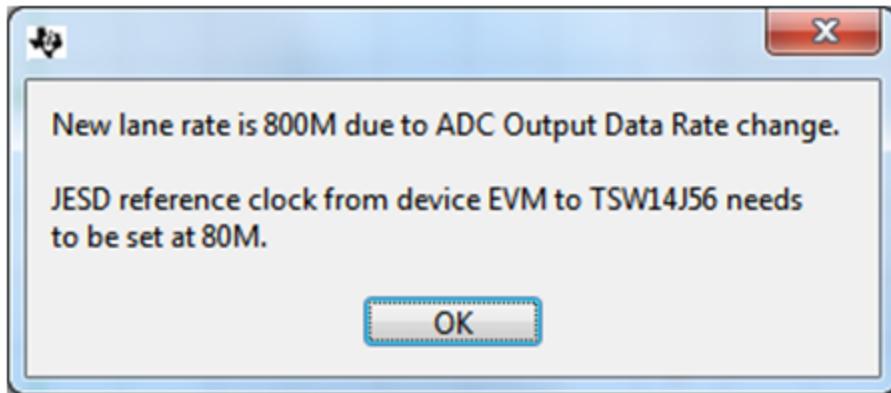


Figure 5. HSDCpro 10x Lane Rate Message

4 Quick Test LVDS Interface

This section outlines the following:

- EVM Layout and Hardware Setup
- How to capture a RAMP and Sinusoidal Inputs for 16ch mode
- How to use scripts to measure all LVDS modes supported by the device

4.1 EVM Layout and Hardware Setup

The ADS52J90 supports 3 modes of operation with respect to the analog inputs: (1) 32-channel mode, (2) 16-channel mode, (3) 8-channel mode. [Figure 6](#) shows the breakdown of the analog channels on the EVM. Testing 32-channel mode is done using all Channels 1-24 on the EVM. Testing 16-channel mode is done using the odd channels of 1-23 on the EVM. These are the vertically-mounted SMAs. Testing 8-channel mode is done using Channels 7 and 8. Channel 7 is configured to accept a differential input to **SMA_CH7A** and **SMA_CH7** whereas Channel 8 is configured to convert a signal ended input to **SMA_CH8** into a differential signal via an amplifier.

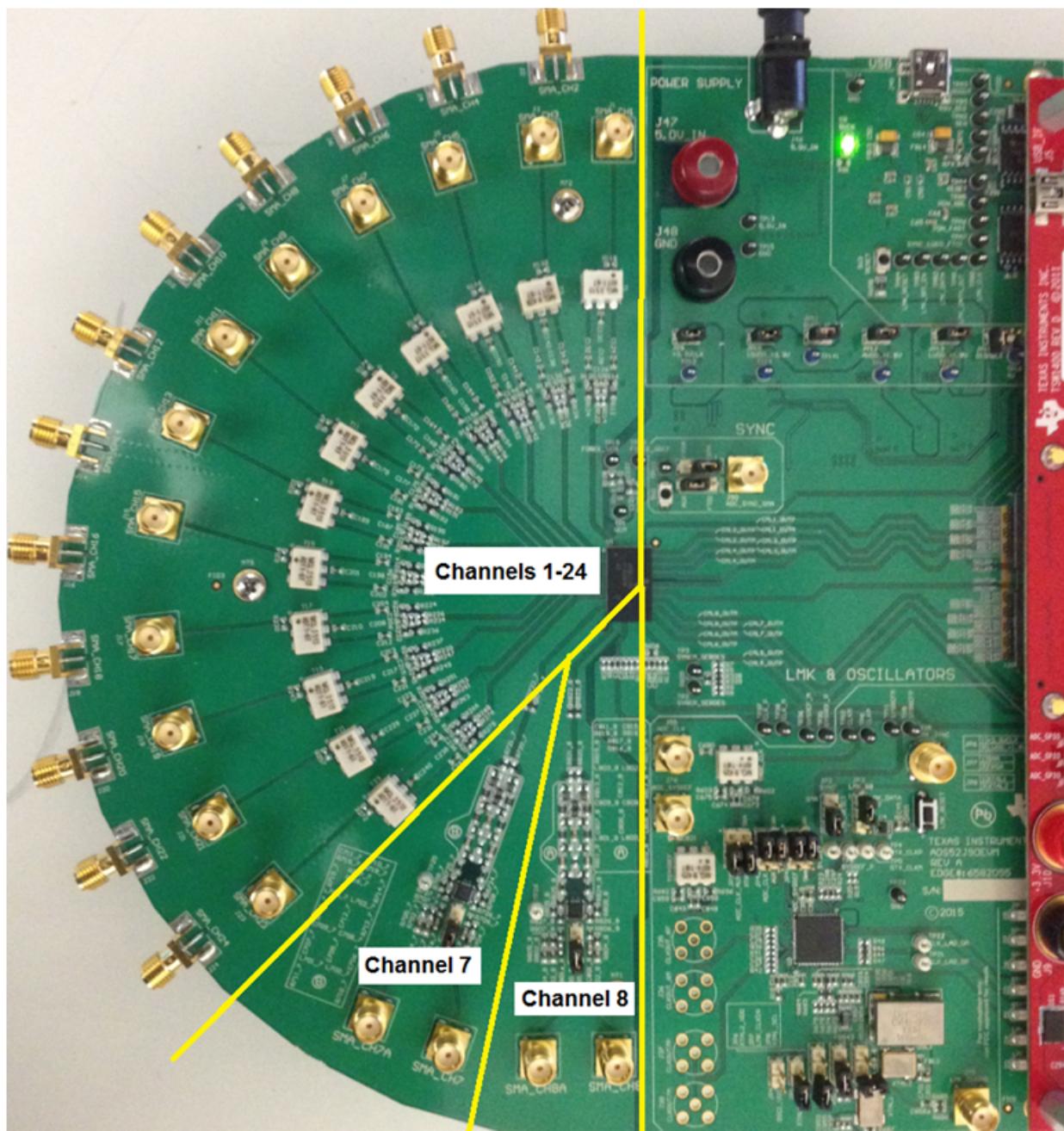


Figure 6. ADS52J90 EVM Analog Channels

The connections shown in [Figure 7](#) should be made for proper hardware setup.

NOTE: Testing the LVDS interface between the ADS52J90 EVM and the TSW1400 EVM can be performed using a RAMP test pattern generated within the ADS52J90 device in lieu of the signal source listed in item 7, in the following steps.

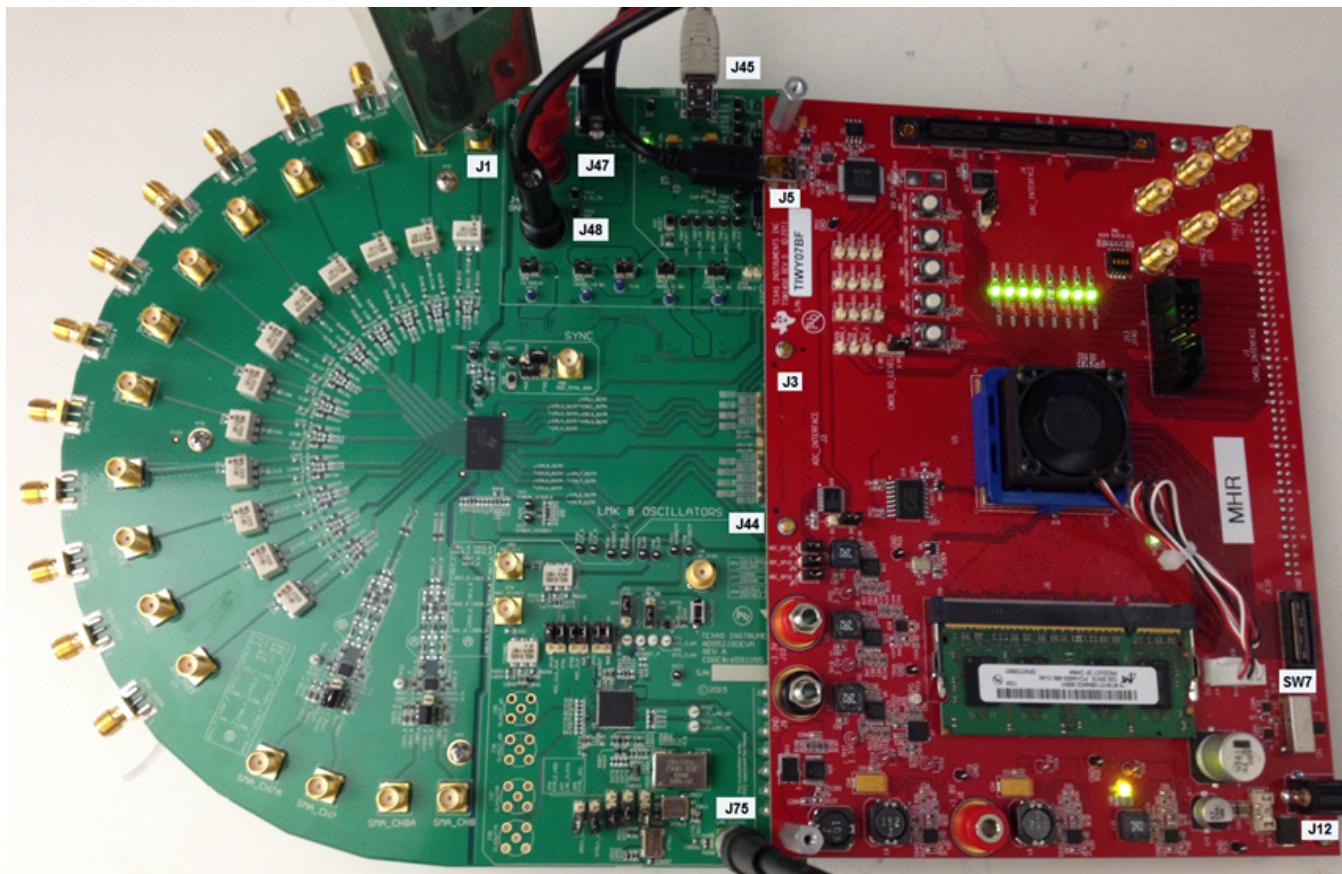


Figure 7. TSW1400 and ADS52J90 Setup

1. Mate the TSW1400 EVM at connector J3 to the ADS52J90 EVM at connector **J44** through the high speed ADC interface connector.

NOTE: The two standoffs closest to J3 on the TSW1400 must be removed. Also, the EVM kit provides two supplementary standoffs that should be added to the remaining two standoffs so that the two EVMs are properly aligned.

2. Connect a DC +5-V power supply output of the provided AC-to-DC power supply to **J12 (+5V_IN)** of the TSW1400 EVM and the input of the power supply cable to a 110–230 VAC source.
3. Ensure that **SW7** is set to ON position on TSW1400.
4. Connect a DC +5-V power supply across banana jacks **J47** and **J48** on the ADS52J90 EVM. Alternatively, test points **TP13** and **TP15** can be used if alligator clip leads are available.
5. Connect the USB cable from the PC to **J45 (USB)** of the ADS52J90 EVM.
6. Connect the USB cable from the PC to **J5 (USB_IF)** of the TSW1400 EVM.

NOTE: TI recommends that the PC USB port be able to support USB2.0. If unsure, always chose the USB ports at the back of the PC chassis over ones located on the front or sides.

7. Supply an analog input signal to SMA J1 (**SMA_CH1**) of the ADS52J90 EVM (such as +16 dBm, 5.0 MHz).

NOTE: A low phase noise signal source (such as R&S SMA100A) with a band pass filter is needed in order to measure SNR values reported in the datasheet. Also, the instrument should have a 10-MHz back panel reference port allowing for coherent sampling when phase locked with the sampling clock signal.

8. Supply a reference clock to SMA J75 (**LMK_CLKIN1**) of the ADS52J90 EVM that is equal to the desired system clock frequency. In the following examples 65 MHz is used as it supports all channel modes of the device.

NOTE: A low phase noise, highly linear, signal source (such as RS SMA100A) is needed in order to measure SNR values reported in the datasheet. Also, the instrument should have a 10-MHz back panel reference port allowing for coherent sampling when phase locked with the analog input clock signal

4.2 Capturing Ramp Test Pattern and Sinusoidal Input

- With the hardware setup shown in [Figure 7](#) established, launch the *High Speed Data Converter Pro GUI*. The GUI should automatically detect the serial number of the TSW1400 EVM connected as shown in [Figure 8](#). Click on OK.

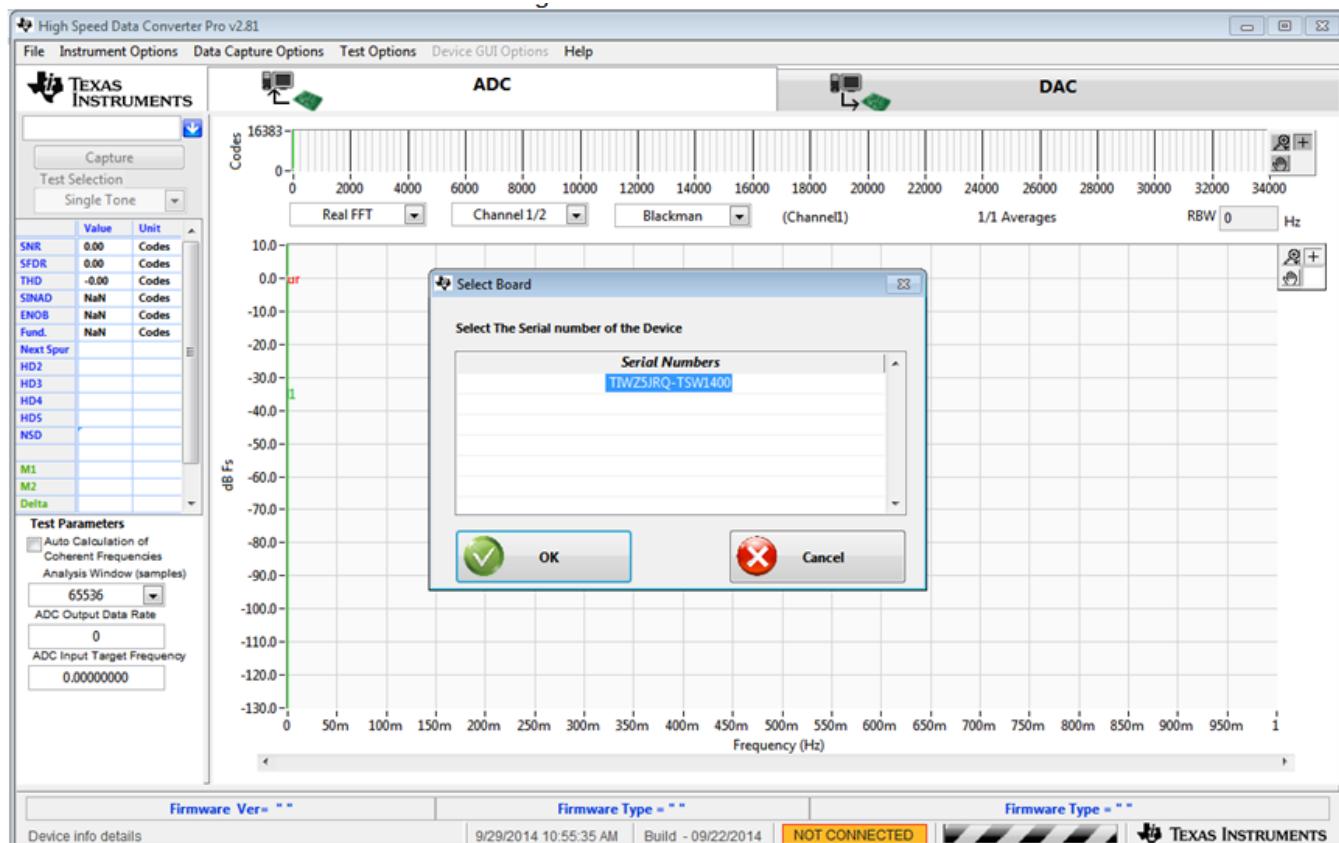


Figure 8. TSW1400 GUI Setup (a)

The message shown in [Figure 9](#) will appear. Click OK.



Figure 9. TSW1400 GUI Setup (b)

If instead, the message shown in [Figure 10](#) appears, it indicates that the USB connection to the TSW1400 EVM is not present. Click OK, then establish a USB connection and repeat [Step 1](#).

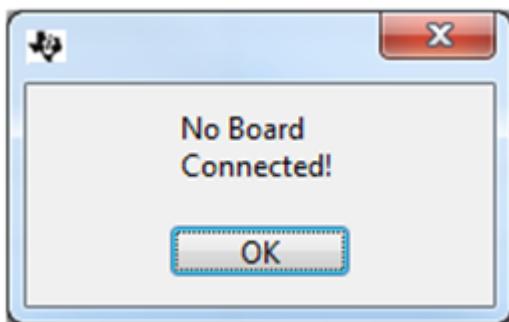


Figure 10. TSW1400 GUI Setup (c)

2. Select a device firmware to load in the FPGA by clicking on the blue arrow in the upper left corner of the HSDCpro GUI. Scroll down and select *ADS52J90* as shown in [Figure 11](#).

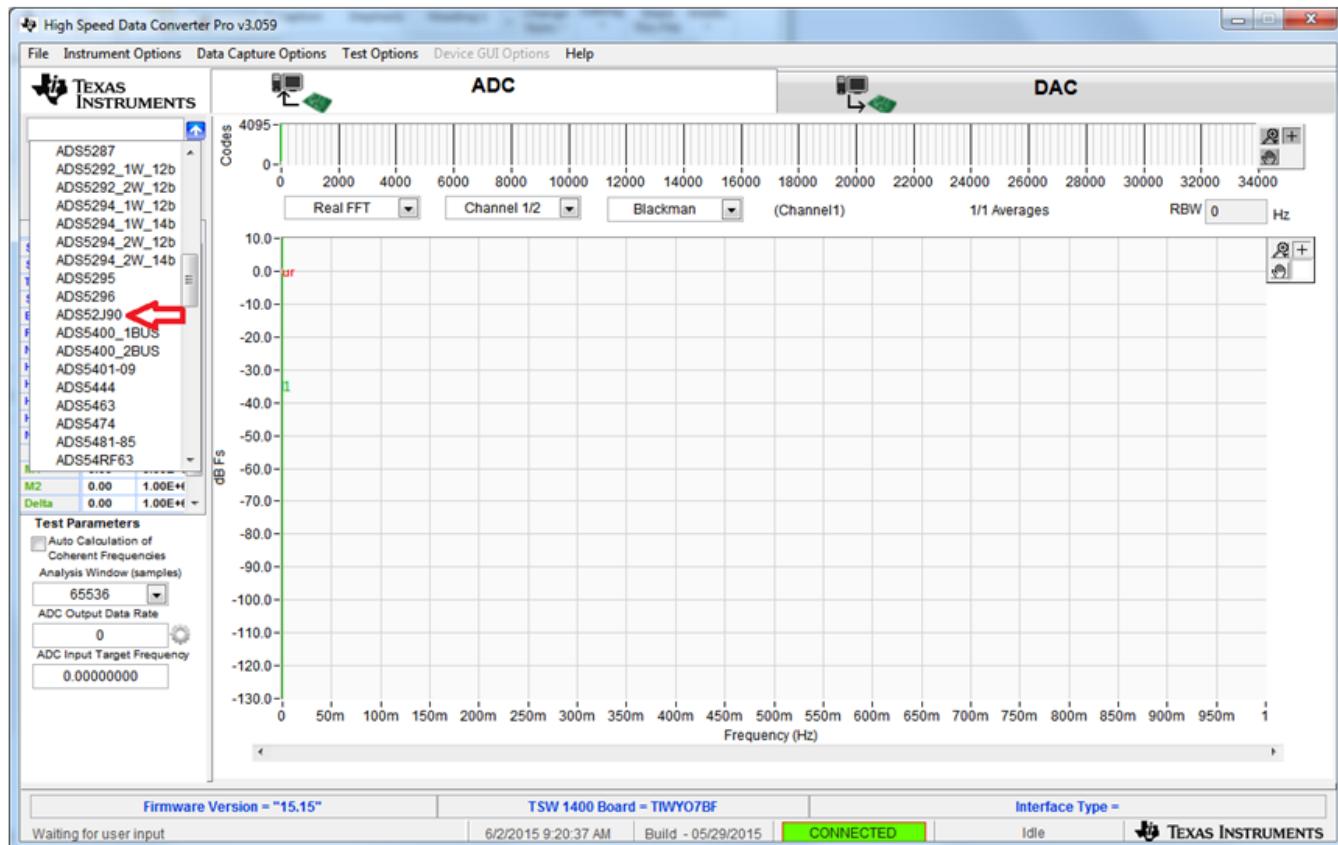


Figure 11. TSW1400 GUI Setup (d)

Click the Yes button to update the ADC firmware on the TSW1400 FPGA as depicted in [Figure 12](#).

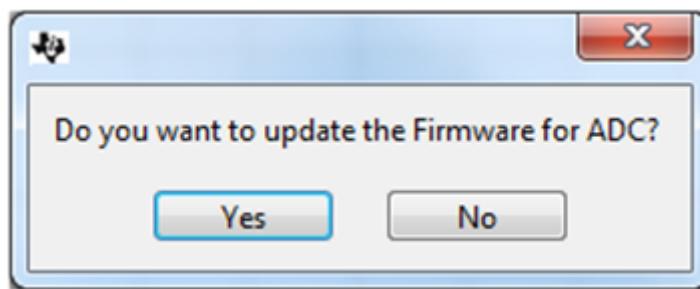


Figure 12. TSW1400 GUI Setup (e)

While the firmware is being loaded into the TSW1400 FPGA, the graphic shown in Figure 13 will appear after which the device GUI (HMC-DAQ) will launch as shown in Figure 14.

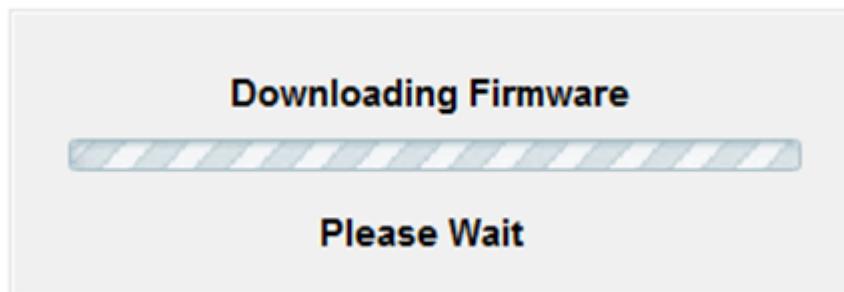


Figure 13. TSW1400 GUI Setup (f)

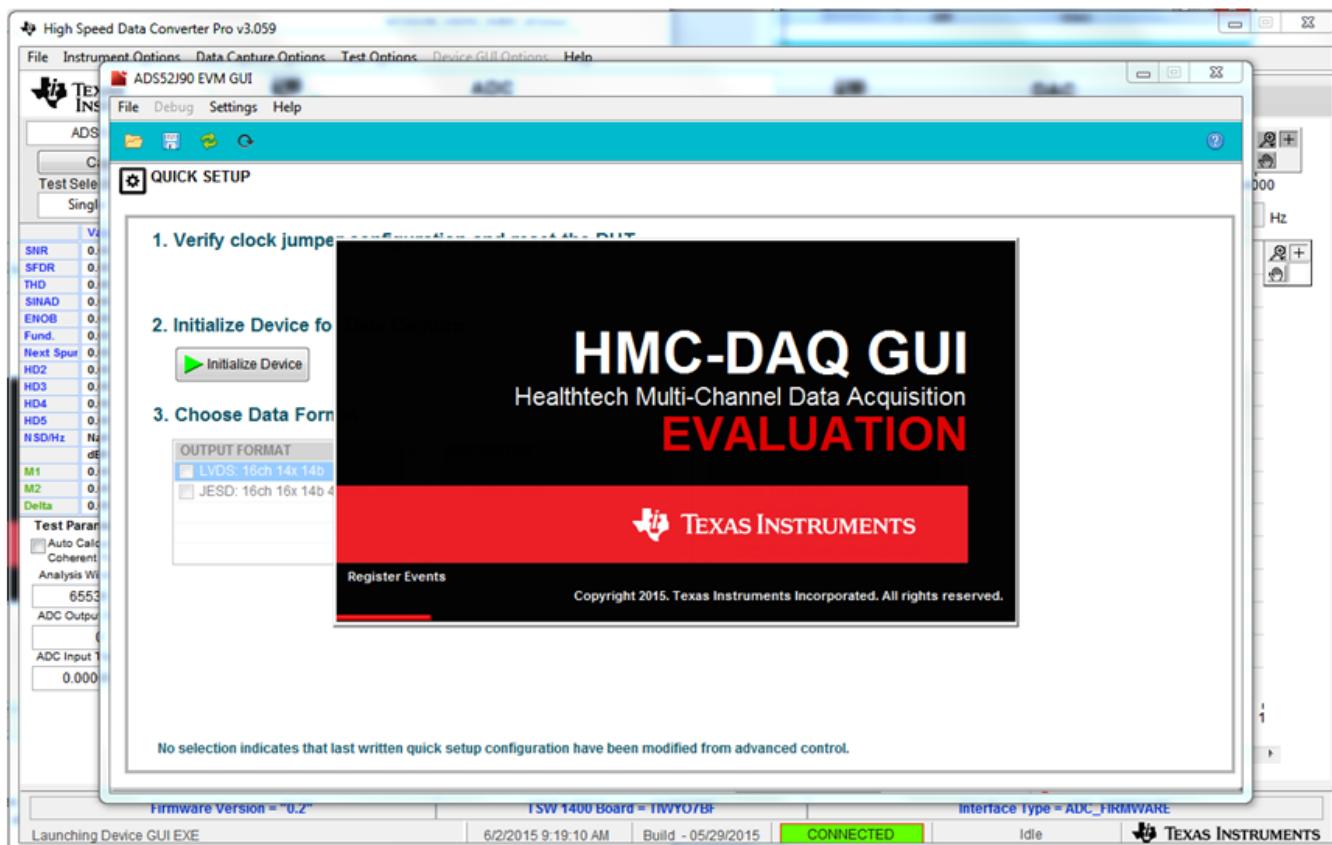


Figure 14. HMC-DAQ GUI Setup (a)

If the GUI recognizes that hardware is connected, HMC-DAQ will show HW CONNECTED in green in the border of the GUI as shown in [Figure 15](#).

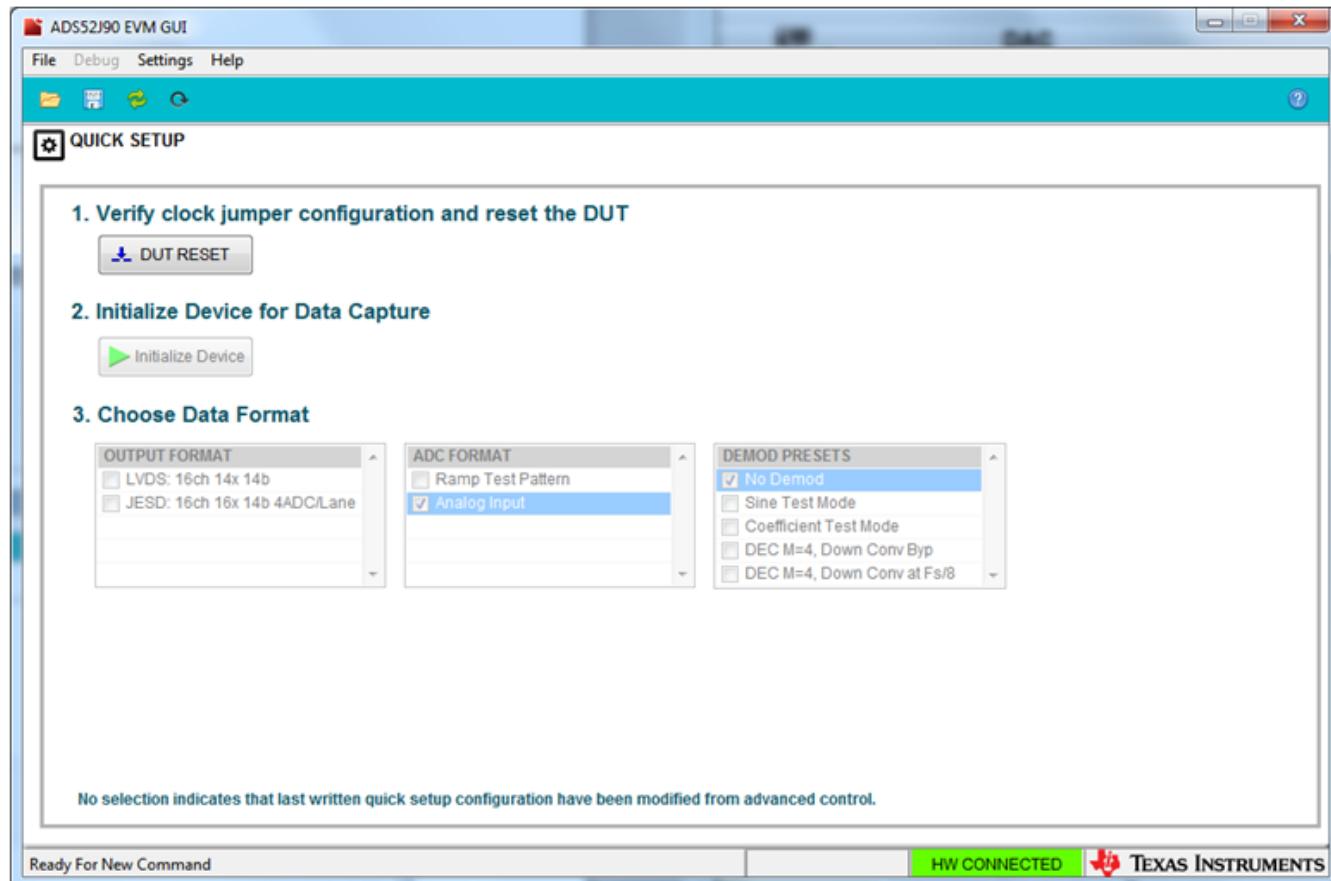


Figure 15. HMC-DAQ GUI Setup (b)

If instead, the message shown in [Figure 16](#) appears, it indicates a USB connection issues between the PC and the ADS52J90 EVM. Close HSDCpro, establish USB connections and restart from [procedure 1](#).

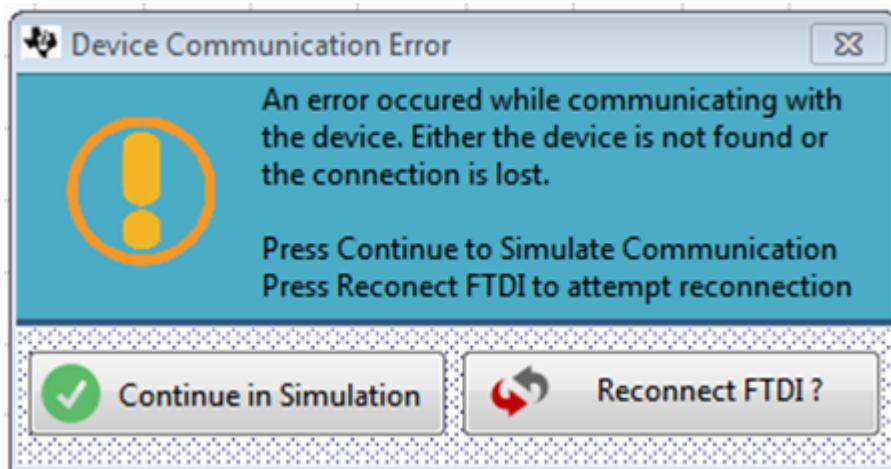


Figure 16. HMC-DAQ GUI Setup (c)

3. At this point there should be two GUI's running and connected, HSDCpro and HMC-DAQ which are communicating behind the scenes. Anytime the ADS52J90 device configuration is updated, HSDCpro is informed and the appropriate firmware updates are done automatically. To capture a RAMP test pattern in LVDS, 16-channel, 14 bit, 14x serialization configuration, do the following as shown in [Figure 17](#):

- a. Press **DUT RESET** button
- b. Press **Initialize Device** button
- c. Check the box next to **LVDS 16ch 14x 14b**
- d. Check the box next to **Ramp Test Pattern**

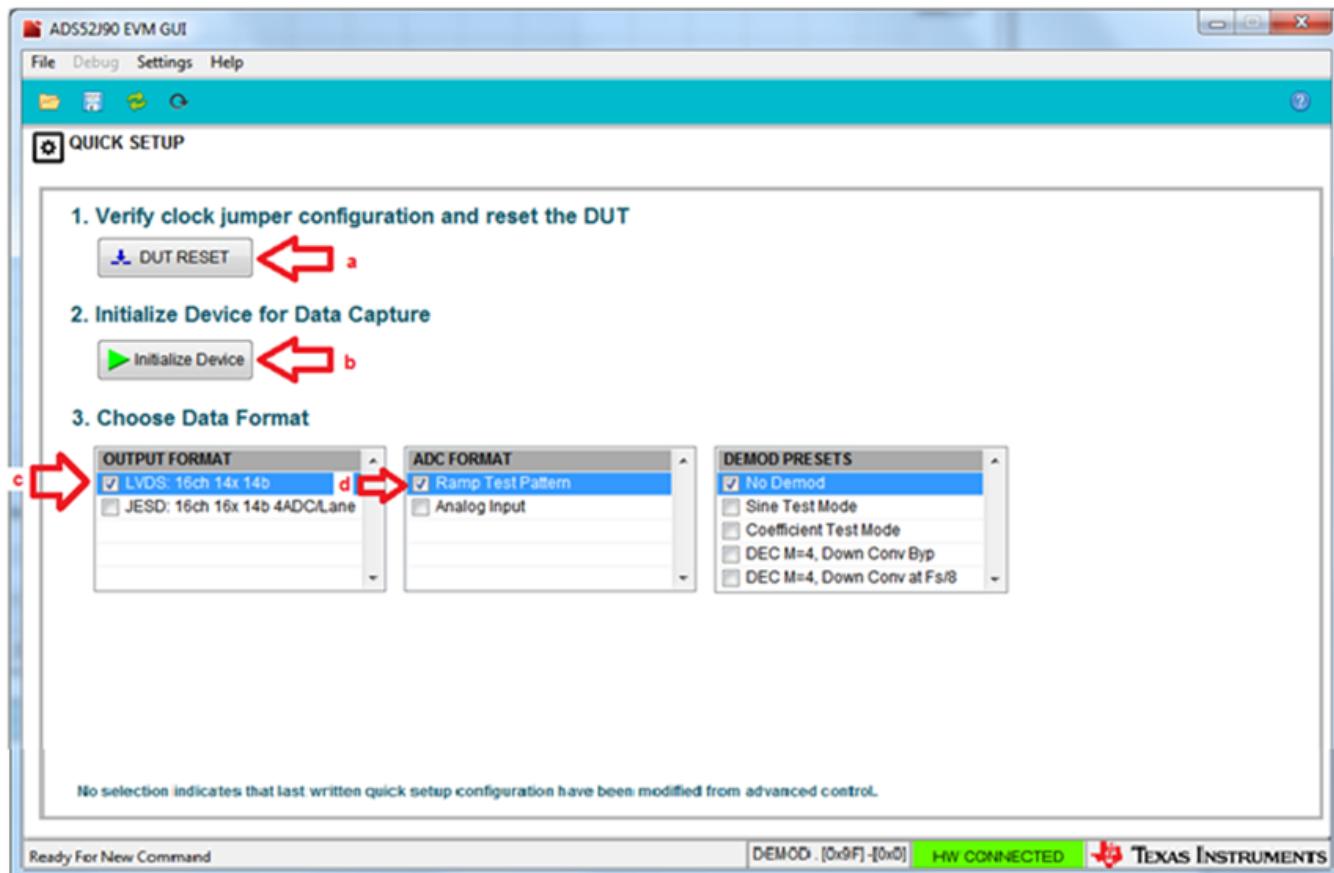


Figure 17. HMC-DAQ GUI Setup (d)

4. Return to HSDCpro GUI and perform the following steps as shown in [Figure 18](#) .
 - a. Change the plot type from *Real FFT* to *Codes*
 - b. Enter 65M in the field labeled *ADC Output Data Rate*
 - c. Press the *Capture* button.

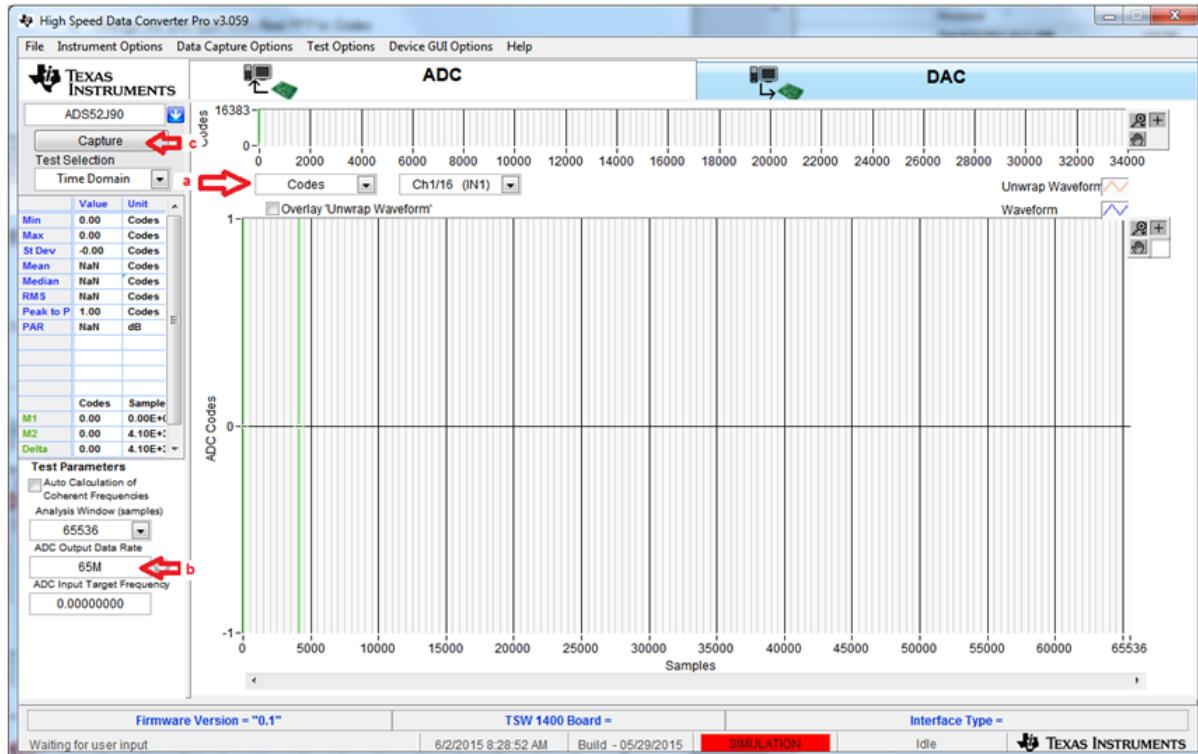


Figure 18. ADS52J90 16-Channel RAMP Capture (a)

A RAMP capture should appear as shown in Figure 19.

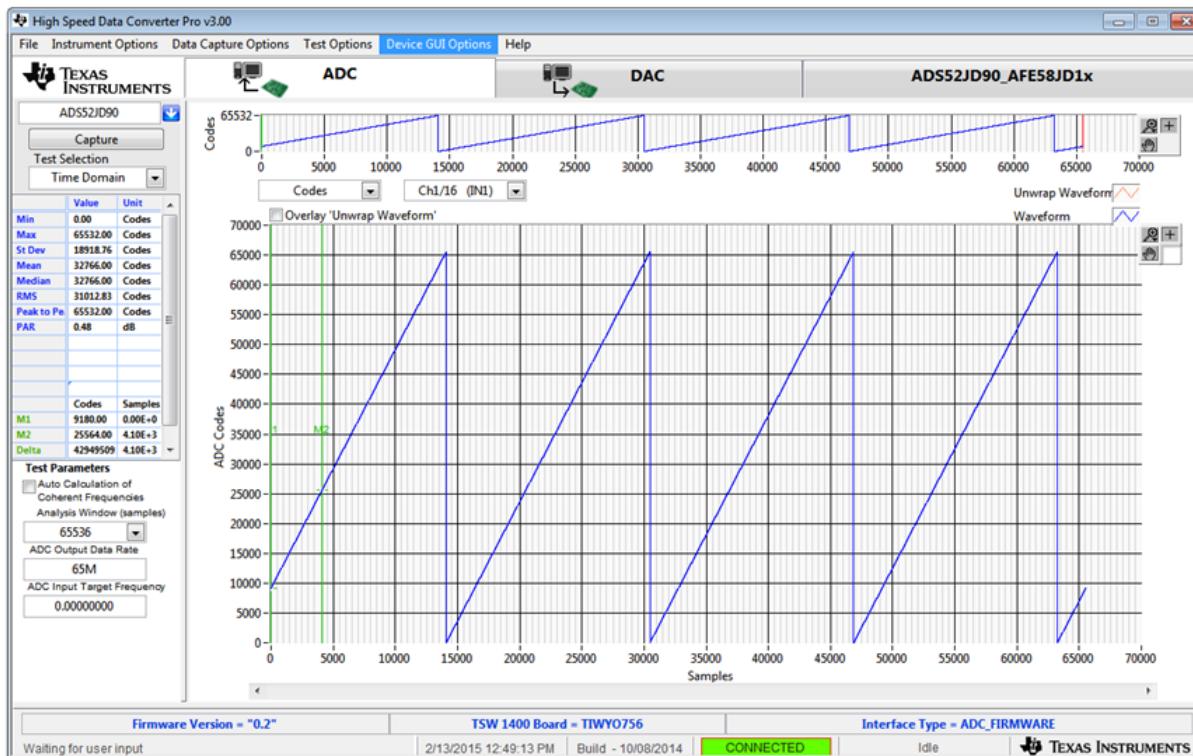


Figure 19. ADS52J90 16-Channel RAMP Capture (b)

By default, *Ch1 (16CH)* is the first channel displayed. Use the drop-down menu shown in Figure 20 to view any one 16 channels.

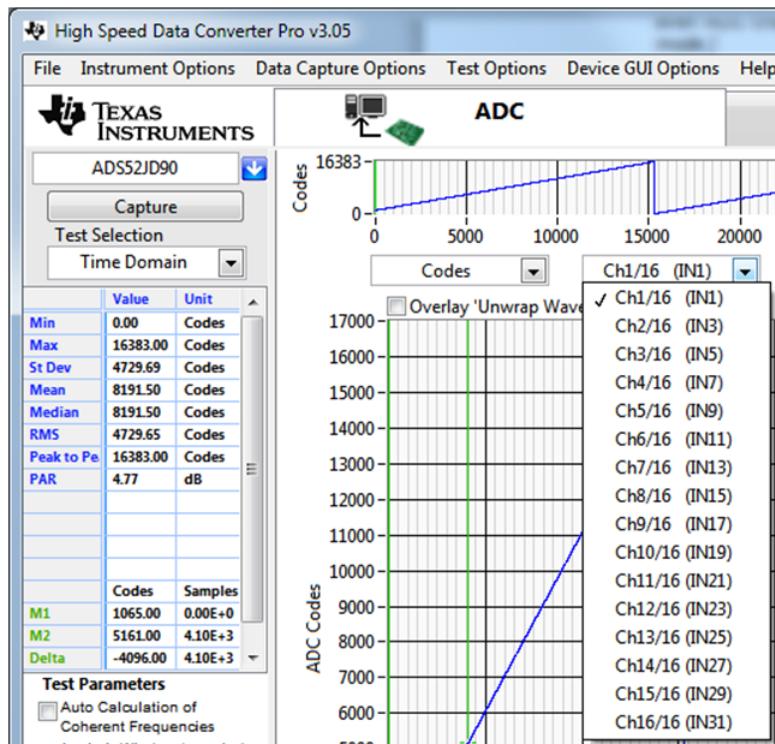


Figure 20. ADS52J90 16-Channel RAMP Capture (c)

Zooming into the waveform and changing the plot graphic (using the buttons to the upper right of graph), as shown in [Figure 21](#), is recommended to confirm that the RAMP waveform is correct with each subsequent sample incremented 1 ADC code until max code of $(2^N) - 1$ is reached, where N is ADC resolution.

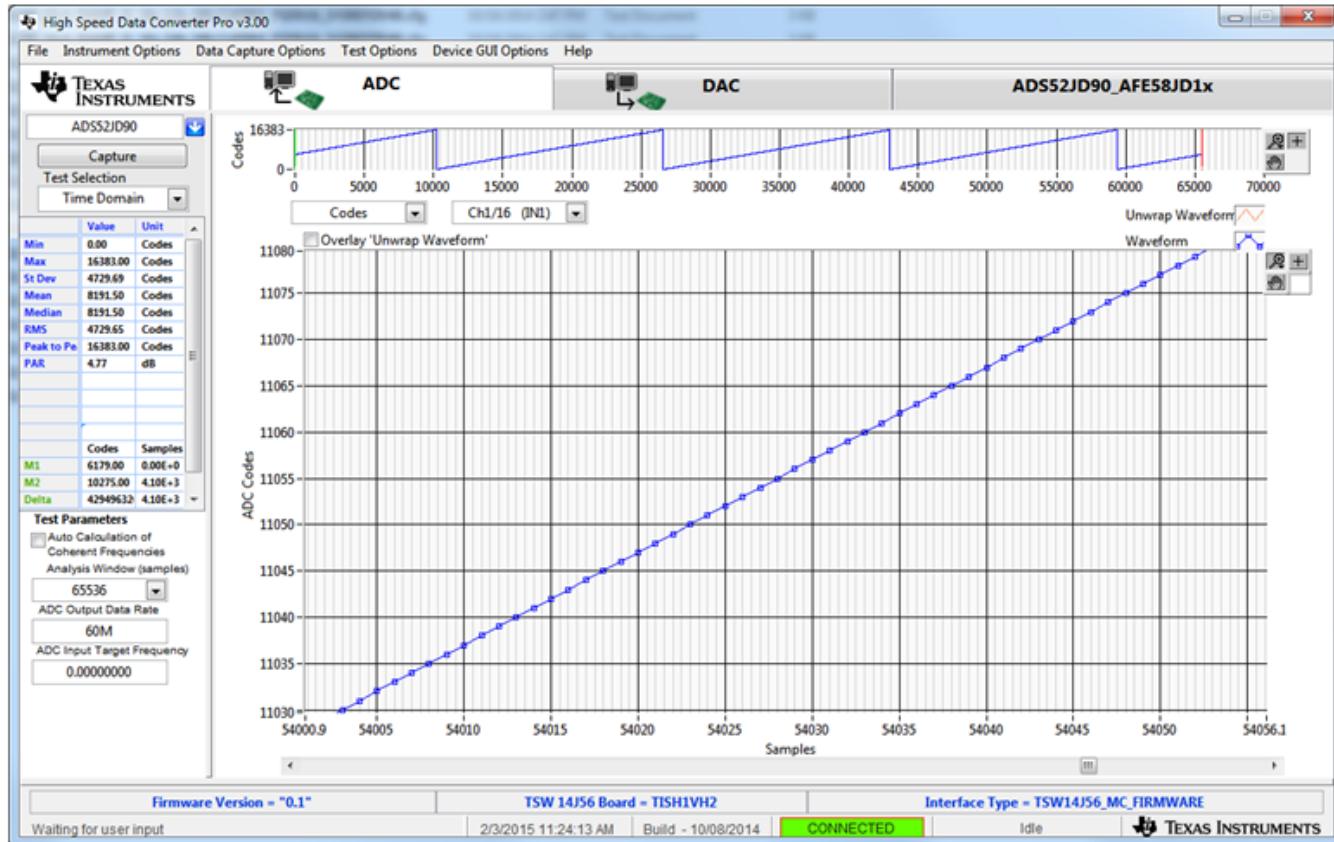


Figure 21. ADS52J90 16-Channel RAMP Capture (d)

5. To capture a sinusoidal input, return to the HMC-DAQ GUI and press the check box next to **Analog Input** as shown in [Figure 22](#).

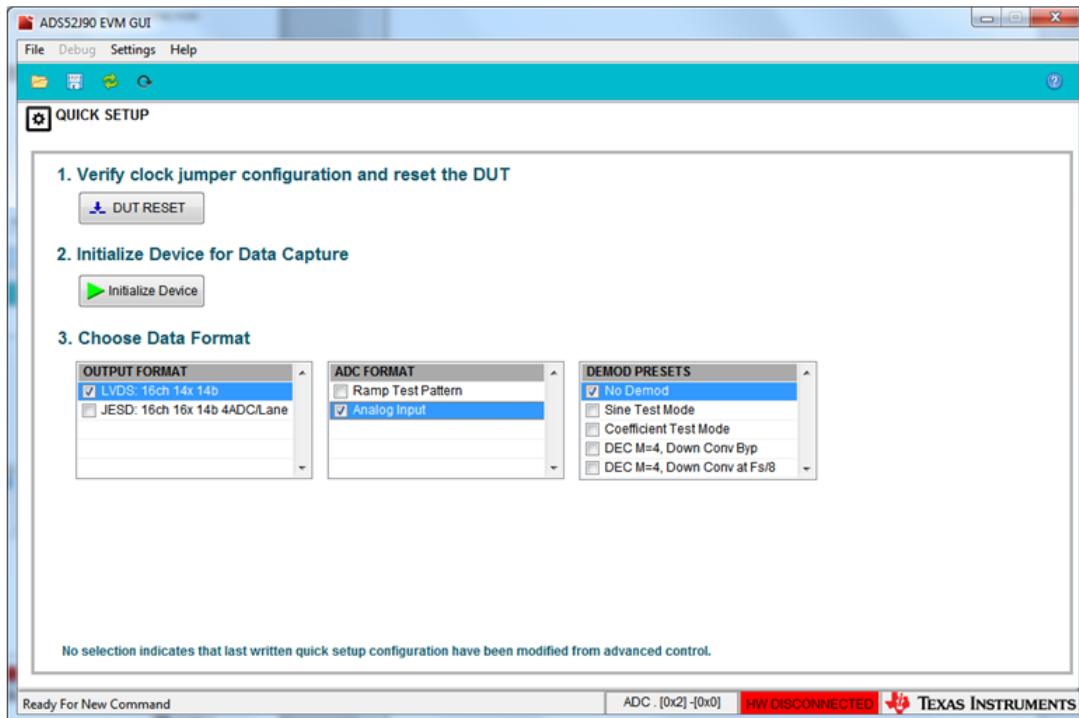


Figure 22. ADS52J90 16-Channel SINE Capture (a)

6. Return to HSDCpro GUI and perform the following (as illustrated in Figure 23):
- Change the plot type from *Codes* to *Real FFT*
 - Enter *65M* in the field labeled *ADC Output Data Rate*
 - Enter *5.0M* in the field labeled *ADC Input Target Frequency* (or set to the desired input that is being provided to SMA J1, **SMA_CH1**, as described in (Section 4.1).
 - Press the *Capture* button.

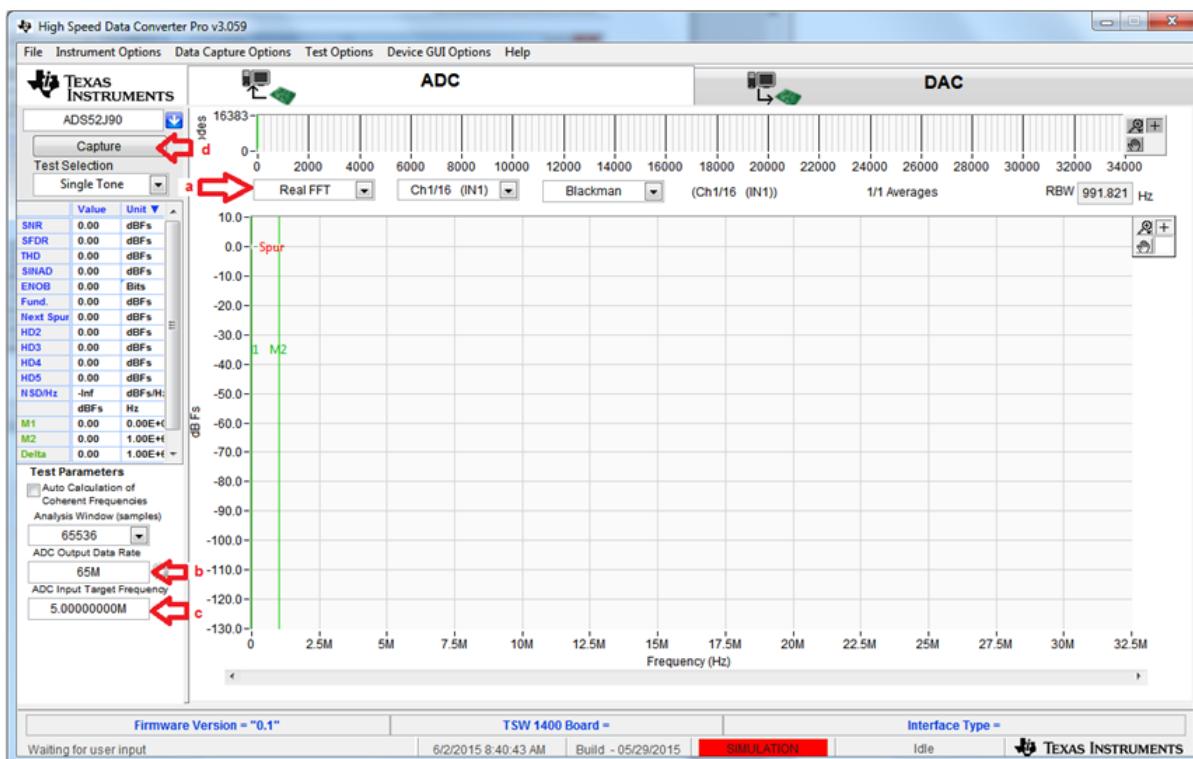


Figure 23. ADS52J90 16-Channel SINE Capture (b)

A capture similar to that shown in [Figure 24](#) should appear.

NOTE: The analog input level was adjusted and a recapture done iteratively until the **Fund.** value was approximately -1 dBFS.

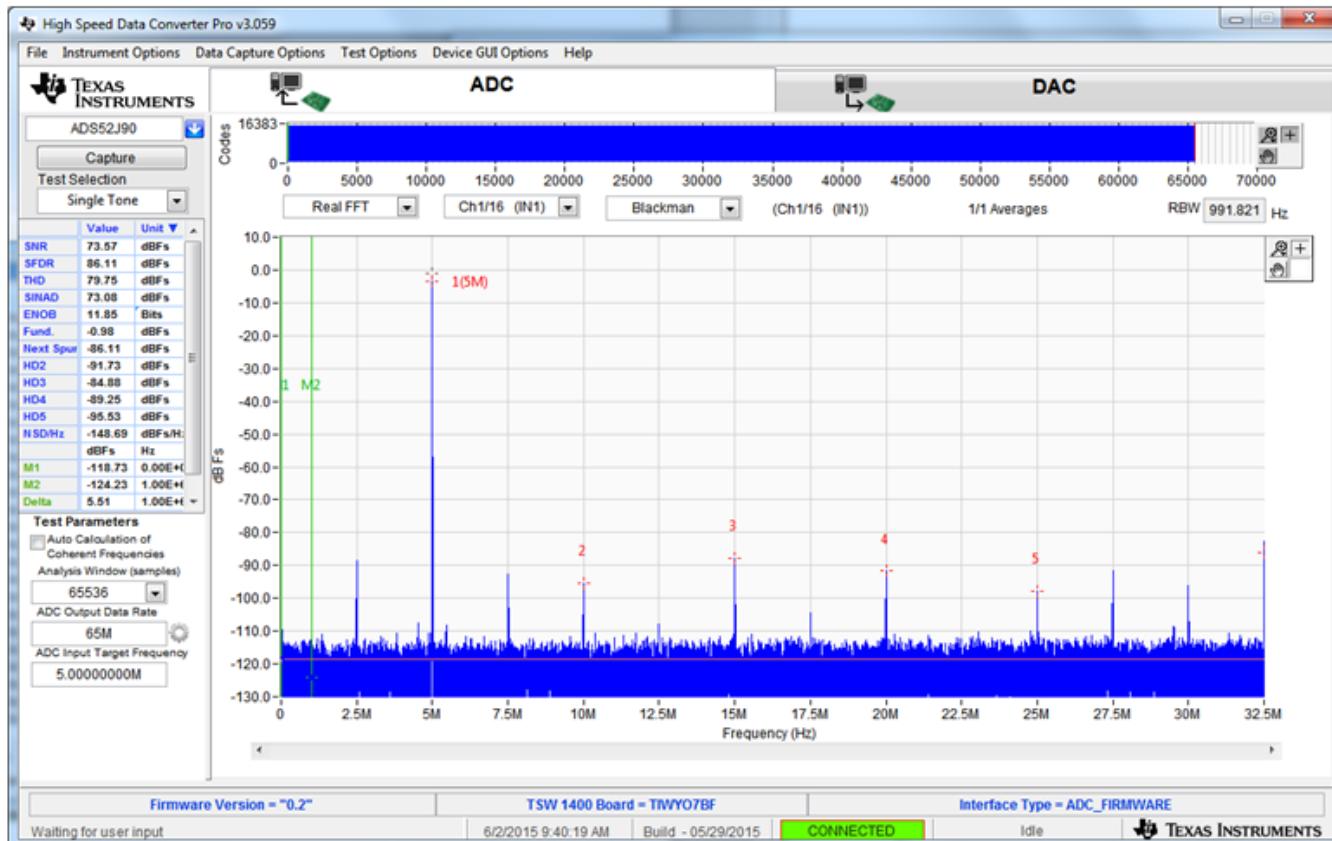


Figure 24. ADS52J90 16-Channel SINE Capture (c)

By default, *Ch1 (16CH)* is the first channel displayed. Use the drop-down menu to view any one 16 channels.

NOTE: The vertically-mounted SMAs on the EVM are the analog inputs to the odd ADC channels while the side-mounted SMAs are the analog inputs to the even ADC channels. Per the datasheet, only odd channels are being sampled when in 16-channel mode.

4.3 Testing All Modes of the Device

In addition to the quick start buttons provided on the **QUICK SETUP** tab of HMC-DAQ GUI, there are scripts to configure the device for all supported modes. To access the scripts, click on the folder icon in the upper left corner of the HMC-DAQ GUI, as shown in [Figure 25](#).

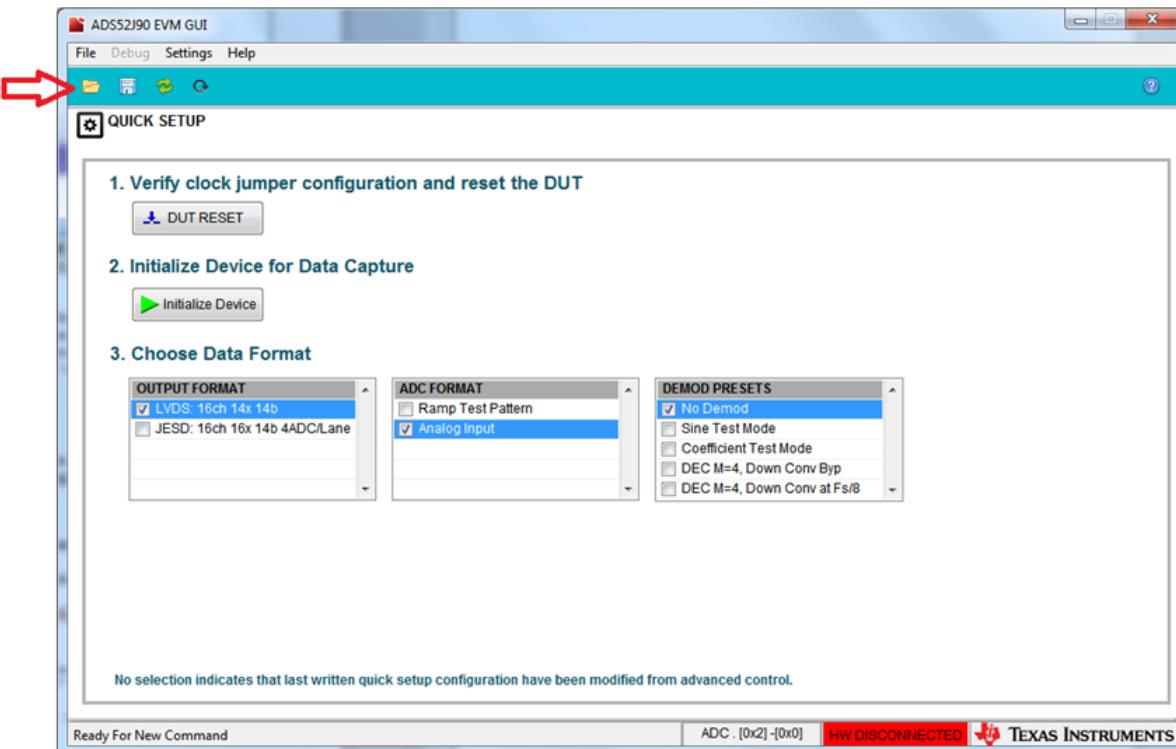


Figure 25. ADS52J90 All Supported Configs

Navigate to the folder/Scripts/ADS52J90/LVDS/LMK_CDM_MODE as shown in [Figure 26](#).

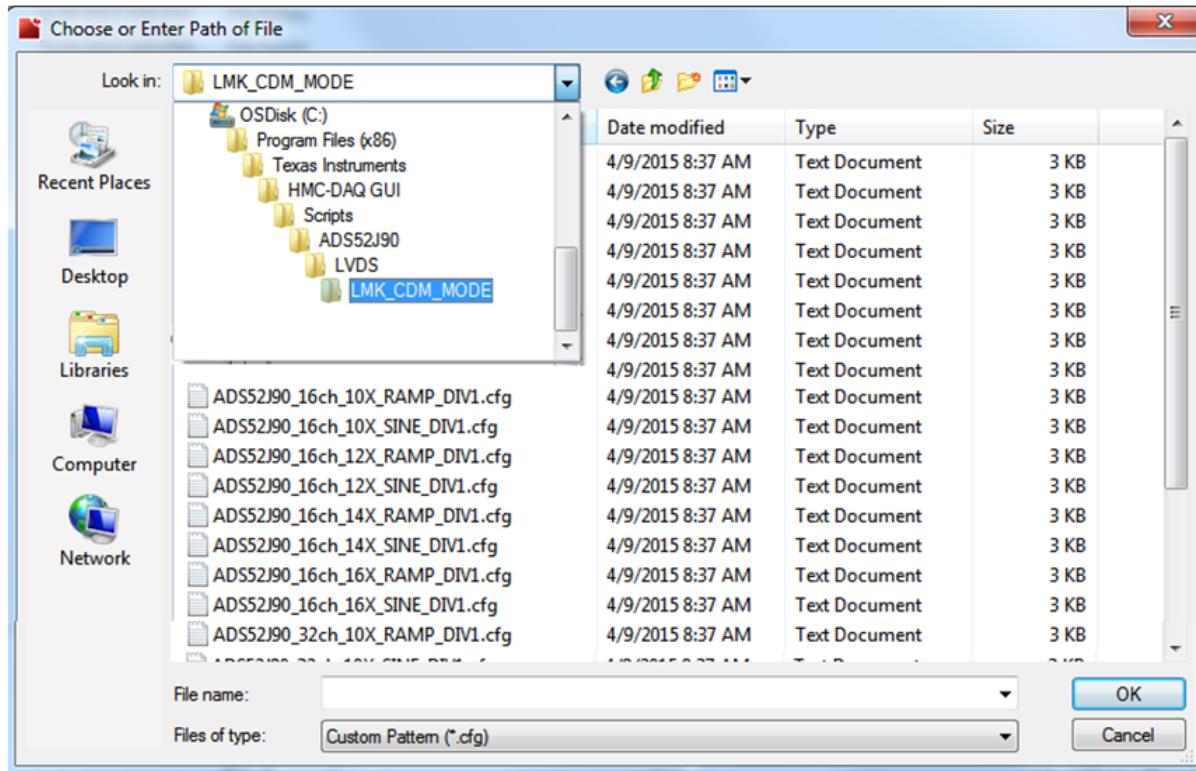


Figure 26. ADS52J90 All Supported Configs (b)

Select anyone of 24 configurations provided and then press *Capture* in HSDCpro. When testing 32-channel mode, ensure that the **ADC Output Data Rate** in HSDCpro is set to half the system clock being provided to the device. For example, if 65 MHz is supplied to **J75** then this value should be set to 32.5 MHz. When testing 8-channel or 16-channel modes, the **ADC Output Data Rate** should be set to the value of the system clock provided to the DUT.

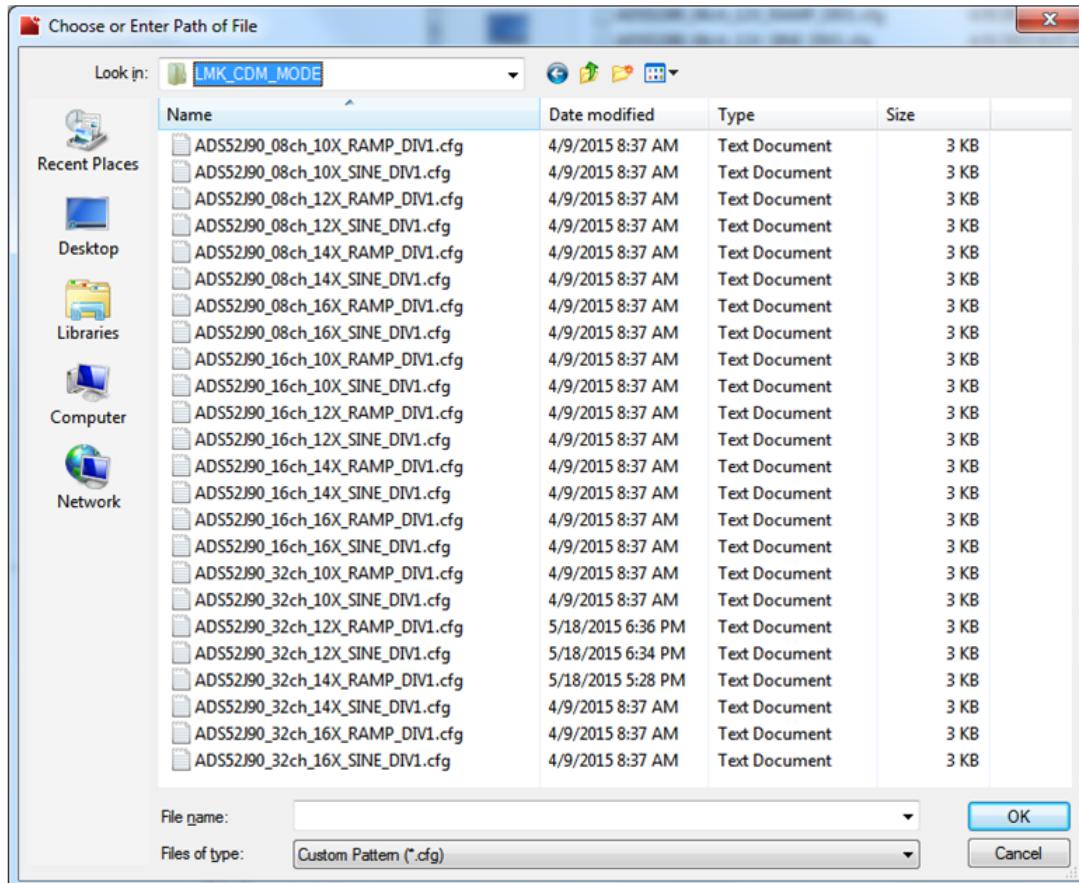


Figure 27. ADS52J90 All Supported Configs (c)

5 Hardware Reference

5.1 Bill of Materials

Table 4. Bill of Materials

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
C1, C2, C4, C9, C12, C32, C70, C77, C85, C94, C103, C112, C117, C285, C286, C297, C298, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C837	34	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata		
C3, C8	2	1uF	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A105KE15D	MuRata		
C5, C10	2	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata		
C6	1	3900pF	CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0402	0402	GRM155R71H392KA01D	MuRata		
C7	1	47pF	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0402	0402	GRM1555C1H470JZ01	MuRata		
C11	1	0.68uF	CAP, CERAMIC, 0.68uF, 6.3V, -20%, +80%, Y5V, 0402	0402	GRM155F50J684ZE01D	MURATA	-	-
C31	1	10uF	CAP, CERAMIC, 10uF, 10V, 10%, X5R, 0603	0603	C1608X5R1A106K080AC	TDK	-	-
C45	1	0.01uF	CAP, CERAMIC, 0.01uF, 50V, 5%, X7R, 0603	0603	06035C103JAT2A	AVX	-	-
C49	1	10uF	CAP, TANT, 10uF, 16V, 10%, 2.8 OHM, 3528-21	3528-21	TAJB106K016RNJ	AVX	-	-
C50, C52, C54	3	4.7uF	CAP, TANT, 4.7uF, 16V, 10%, 4 OHM, 3216-18	3216-18	TAJA475K016RNJ	AVX	-	-
C51, C55, C289, C290, C291, C292	6	0.1uF	CAP, CERAMIC, 0.1uF, 16V, 10%, X5R, 0402	0402	EMK105BJ104KV-F	TAIYO YUDEN	-	-
C53	1	0.01uF	CAP, CERM, 0.01uF, 25V, +/-10%, X7R, 0402	0402	GRM155R71E103KA01D	MuRata		
C56, C57	2	100uF	CAP, CERAMIC, 100uF, 6.3V, 20%, X5R, 1206	1206	C1206C107M9PACTU	KEMET	-	-
C58, C853	2	10uF	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	0603	GRM188R60J106ME47D	MuRata		
C61, C62	2	27pF	CAP, CERAMIC, 27pF, 250V, 2%, NPO, 0603	0603	251R14S270GV4T	JOHANSON TECHNOLOGY INC	-	-
C63, C64, C65, C66, C67, C68, C69, C700_7, C701_7, C701a_7, C800_8, C801_8	12	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	0603	GRM188R71C104KA01D	MuRata		
C72, C82, C96, C98, C107, C114, C116, C120	8	1uF	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603	0603	C1608X7R1E105K080AB	TDK		
C73, C97, C115	3	47uF	CAP, CERAMIC, 47uF, 10V, 20%, X5R, 1206	1206	GRM31CR61A476ME15L	MURATA	-	-
C74, C79, C102, C111	4	10uF	CAP, CERAMIC, 10uF, 25V, 10%, X5R, 0805	0805	GRM21BR61E106KA73L	MURATA	-	-
C75, C76, C83, C84	4	0.01uF	CAP, CERM, 0.01uF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A103KA01D	MuRata		
C78	1	47uF	CAP, TA, 47uF, 10V, +/-10%, 0.25 ohm, SMD	3528-21	TPSB476K010R0250	AVX		
C80, C86, C104, C118	4	33uF	CAP, TA, 33uF, 16V, +/-10%, 0.35 ohm, SMD	3528-21	TPSB336K016R0350	AVX		
C81, C87, C105, C119	4	10uF	CAP, CERAMIC, 10uF, 6.3V, 20%, X5R, 0805	0805	C2012X5R0J106M125AB	TDK CORPORATION	-	-
C88	1	0.1uF	CAP, CERAMIC, 0.1uF, 10V, 10%, X5R, 0402	0402	C0402C104K8PAC	KEMET	-	-
C89, C90	2	22uF	CAP, TA, 22uF, 16V, +/-10%, 0.375 ohm, SMD	6032-28	TPSC226K016R0375	AVX		
C92	1	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1206	1206	GRM31CR61E106KA12L	MuRata		
C93, C106	2	0.1uF	CAP, CERAMIC, 0.1uF, 16V, 10%, X7R, 0603	0603	0603YC104KAT2A	AVX	-	-
C99, C100, C101	3	22uF	CAP, CERM, 22uF, 10V, +/-20%, X5R, 1210	1210	C3225X5R1A226M	TDK		

Table 4. Bill of Materials (continued)

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
C109	1	0.01uF	CAP, CERAMIC, 0.01uF, 25V, 10%, X7R, 0603	0603	C1608X7R1E103K080AA	TDK	-	-
C110	1	3300pF	CAP, CERAMIC, 3300pF, 50V, 10%, X7R, 0603	0603	06035C332KAT2A	AVX	-	-
C121	1	1uF	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	0603	C0603C105K8PACTU	Kemet		
C122, C123, C124, C127, C128, C129, C130, C131, C132, C133, C134, C137, C138, C139, C140, C141, C142, C143, C144, C147, C148, C149, C150, C151, C152, C153, C154, C157, C158, C159, C160, C161, C162, C163, C164, C167, C168, C169, C170, C171, C172, C173, C174, C177, C178, C179, C180, C181, C182, C183, C184, C187, C188, C189, C190, C191, C192, C193, C194, C197, C198, C199, C200, C201, C202, C203, C204, C207, C208, C209, C210, C211, C212, C213, C214, C217, C218, C219, C220, C221, C222, C223, C224, C227, C228, C229, C230, C231, C232, C233, C234, C237, C238, C239, C240, C241, C242, C673, C674, C675, C678, C680, C821, C848, C849, C858, C858a, C859	108	0.1uF	'CAP, CERAMIC, 0.1uF, 16V, 10%, X7R, 0402	402	0402YC104KAT2A	AVX		
C701	1	1000pF	CAP, CERAMIC, 1000pF, 50V, 10%, X7R, 0402	0402	ECJ-0EB1H102K	PANASONIC	-	-
C702_7, C703_7, C704_7, C802_8, C803_8, C804_8	6	0.22uF	CAP, CERM, 0.22 μ F, 25 V, +/- 10%, X5R, 0603	0603	06033D224KAT2A	AVX		
C706_7, C707_7, C806_8, C807_8	4	0.01uF	CAP, CERM, 0.01 μ F, 50 V, +/- 10%, X7R, 0603	0603	C1608X7R1H103K	TDK		
C712_7, C812_8	2	0.1uF	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX		
C713_7, C813_8	2	33pF	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	0603	GRM1885C1H330JA01D	MuRata		
C801	1	10uF	CAP, CERAMIC, 10uF, 6.3V, 20%, X5R, 0603	0603	JMK107BJ106MA-T	TAIYO YUDEN	-	-
C830, C833, C838	3	0.1uF	CAP, CERAMIC, 0.1uF, 16V, 10%, X7R, 0402	0402	GRM155R71C104KA88	MURATA	-	-
C850, C851	2	0.01uF	CAP, CERM, 0.01uF, 25V, +/-10%, X7R, 0402	0402	C1005X7R1E103K	TDK		
C854, C855	2	100pF	CAP, CERAMIC, 100pF, 50V, 5%, C0G, 0402	0402	GRM1555C1H101JZ01D	MURATA	-	-
C856	1	10pF	CAP, CERAMIC, 10pF, 50V, 5%, C0G, 0402	0402	GRM1555C1H100JZ01D	MURATA	-	-
C857	1	2200pF	CAP, CERAMIC, 2200pF, 50V, 10%, X7R, 0402	0402	GRM155R71H222KA01D	MURATA	-	-
D1, D2, D3, D4, D5, D6, D7, D8	8	GREEN	LED, GREEN CLEAR, 1206 SMD	1206	LTST-C150KGKT	LITE-ON INC	-	-
D9	1	15V	Diode, Schottky, 15V, 25A, DDPAK	DDPAK	MBRB2515LT4G	ON Semiconductor		
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB543	10	120	FERRITE BEAD, 120 OHM, 25% , 3500 mA, 0.02 OHM, SMT-1206	1206	BLM31PG121SN1L	MURATA	-	-
FB10	1	1K	FERRITE BEAD, 1K OHM, 25% , 200 mA, 0.65 OHM, SMT-0402	0402	BLM15AG102SN1D	MURATA	-	-
FB13, FB14, L2, L3	4	120 ohm	Ferrite Bead, 120 ohm @ 100 MHz, 4 A, 1206	1206	HII206P121R-10	Laird-Signal Integrity Products		
FB15	1	80 OHM	FERRITE BEAD, 80 OHM AT 100 MHZ, 5A, 0.01 OHM, SMT0805	0805	HII0805R800R-10	LAIRD TECH	-	-
FB16, FB17	2		FILTER, LC HIGH FREQ, 27UF, SMD 1206	1206	NFM31PC276B0J3	MURATA	-	-
H1, H2	2		HEX STANDOFF 6-32 ALUMINUM 1/2	Standoff	8414	Keystone	-	-

Table 4. Bill of Materials (continued)

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
J1, J3, J5, J7, J7_7, J7a_7, J8_8, J8a_8, J9, J11, J13, J15, J17, J19, J21, J23	16		Connector, 50 OHM, TH, SMA, ROHS	-	SMA-J-P-H-ST-TH1	SAMTEC	-	-
J2, J4, J6, J8, J10, J12, J14, J16, J18, J20, J22, J24	12		CONNECTOR, SMA JACK, 50 OHM, EDGE MOUNT	-	142-0711-821	EMERSON CONNECTIVITY	-	-
J39	1		Connector, TH, SMA	SMA	142-0701-201	Emerson Network Power		
J43	1		Connector, Receptacle, 400-Pos (40x10), 50x50-mil Pitch, SMT	2196x280x478 mil	ASP-134488-01	Molex	45970-4315	Molex
J44	1		CONNECTOR, HEADER, 120 POS, SMT	-	QTH-060-02-F-D-A	SAMTEC	-	-
J45	1		Connector, Receptacle, USB - mini AB, R/A, SMD	Receptacle, 5-Leads, Body 9.9x9mm, R/A	67803-8020	Molex		
J46	1		Power Jack, mini, 2.1mm OD, R/A, TH	Jack, 14.5x11x9mm	RAPC722X	Switchcraft		
J47	1		BANANA JACK, INSULATED, SOLDER LUG, RED COLOR, TH-1P	-	SPC15363	TENMA		-
J48	1		BANANA JACK, INSULATED, SOLDER LUG, BLACK COLOR, TH-1P	-	SPC15354	TENMA		-
J50, J55, J75, J76	4		CONN, SMA, JACK, 2.54 MM PITCH, STRAIGHT, THRU	-	901-144-8RFX	AMPHENOL	-	-
JP2, JP3, JP6, JP7, JP8, JP28, JP33, JP700_7, JP800_8	9		CONN, HEADER, 3POS, .100", T/H GOLD	-	HTSW-103-07-G-S	SAMTEC	-	-
JP4, JP5, JP9, JP10, JP11, JP12, JP13	7		CONN, MALE, STRAIGHT, 2.54 MM PITCH, 2-PIN, THRU	-	HMTSW-102-07-G-S-240	SAMTEC	-	-
JP39, JP40, JP41	3		Header, TH, 100mil, 3x2, Gold plated, 230 mil above insulator	3x2 Header	TSW-103-07-G-D	Samtec		
L1	1	1K OHM	FERRITE CHIP, EMIFIL, 1K OHM AT 100 MHZ, 500mA, 0.28 ohm, SMT0805	0805	BLM21AG102SN1D	MURATA	-	-
L4	1	1.5uH	Inductor, Shielded, Composite, 1.5uH, 7.12A, 0.02 ohm, SMD	4x2.1x4mm	XAL4020-152MEB	Coilcraft		
MT1, MT2, MT3, MT4, MT5	5		Threaded Standoffs	-	2205	KEYSTONE	-	-
OSC1	1	100.00 MHZ	OSCC, VCXO CMOS, 100.0 MHZ ,3.3V, +/-20ppm, SMT, 4P	-	CVHD-950-100.000	CRYSTEK CORPORATION	-	-
Q1	1	30V	MOSFET, N-CH, 30V, 5A, SON 2x2mm	SON 2x2mm	CSD17313Q2	Texas Instruments		None
R13, R14, R91	3	1K OHM	RESISTOR, THICK FILM, 1K OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF1001X	PANASONIC	-	-
R16	1	620	RESISTOR, THICK FILM, 620 OHM, 5%, 0.1W, SMT0402	0402	ERJ-2GEJ621X	PANASONIC	-	-
R18	1	39K	RESISTOR, THICK FILM, 39K OHM, 5%, 0.1W, SMT0402	0402	ERJ-2GEJ393X	PANASONIC	-	-
R39, R40, R43, R45, R61, R63, R64	7	750	RES, 750 ohm, 1%, 0.1W, 0603	0603	CRCW0603750RFKEA	Vishay-Dale		
R44, R46, R88, R90, R92, R93, R95, R338, R339, R592, R593, R595, R687	13	0	RESISTOR, THICK FILM, 0 OHM, JUMPER, 0.1W, SMT0402	0402	ERJ-2GE0R00X	Panasonic		
R55, R75, R79, R80, R81	5	10K OHM	RESISTOR, THICK FILM, 10K OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF1002X	PANASONIC	-	-
R67, R68	2	10.0	RES, 10.0 ohm, 1%, 0.1W, 0603	0603	RC0603FR-0710RL	Yageo America		

Table 4. Bill of Materials (continued)

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
R71	1	12K	RESISTOR, THICK FILM, 12K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF1202V	PANASONIC	-	-
R72	1	4.7K OHM	RESISTOR, THICK FILM, 4.7K OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF4701X	PANASONIC	-	-
R74	1	1K	RESISTOR, THICK FILM, 1K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF1001V	PANASONIC	-	-
R84	1	2.2K OHM	RESISTOR, THICK FILM, 2.2K OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF2201X	PANASONIC	-	-
R96	1	30k	RES, 30 ohm, 5%, 0.063W, 0402	0402	CRCW040230K0JNED	Vishay-Dale		
R98, R102	2	100K	RESISTOR, THICK FILM, 100K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF1003V	PANASONIC	-	-
R103	1	26.1K	RESISTOR, THICK FILM, 26.1K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF2612V	PANASONIC	-	-
R104	1	665K	RESISTOR, THICK FILM, 665K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF6653V	PANASONIC	-	-
R105	1	7.68K	RESISTOR, THICK FILM, 7.68K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF7681V	PANASONIC	-	-
R110, R111, R112, R123, R124, R125, R126, R137, R138, R139, R140, R151, R152, R153, R154, R165, R166, R167, R168, R179, R180, R181, R182, R193, R194, R195, R196, R207, R208, R209, R210, R221, R222, R223, R224, R235, R236, R237, R238, R249, R250, R251, R252, R263, R264, R265, R266, R277, R278, R822_8, R823_8	51	10.0	RES, 10.0 ohm, 1%, 0.063W, 0402	0402	CRCW040210R0FKED	Vishay-Dale		
R115, R116, R119, R120, R129, R130, R133, R135, R143, R144, R147, R148, R157, R158, R161, R162, R171, R172, R175, R177, R185, R186, R189, R190, R199, R200, R203, R205, R212, R214, R217, R219, R227, R228, R231, R232, R241, R242, R245, R246, R255, R256, R259, R260, R269, R270, R273, R274	48	24.9	RES, 24.9 ohm, 1%, 0.063W, 0402	0402	CRCW040224R9FKED	Vishay-Dale		
R520, R521, R524, R525, R686	5	49.9	RESISTOR, THICK FILM, 49.9 OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF49R9X	PANASONIC	-	-
R602, R603, R682, R683, R684, R696	6	100	RESISTOR, THICK FILM, 100 OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF1000X	PANASONIC	-	-
R604, R605, R606	3	100	RES, 100 ohm, 5%, 0.063W, 0402	0402	CRCW0402100RJNED	Vishay-Dale		
R634, R698	2	10k	RES, 10k ohm, 5%, 0.125W, 0805	0805	ERJ-6GEYJ103V	Panasonic		
R685	1	0	RESISTOR, THICK FILM, 0 OHM, JUMPER, 0.063W, SMT0402	0402	CRCW04020000Z0ED	VISHAY	-	-
R706_7, R707_7	2	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R708_7, R709_7, R722_7, R723_7, R824_8, R825_8, R826_8, R827_8	8	0	RES, 0, 1%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America		
R710_7, R711_7, R810_8, R811_8	4	15.0	RES, 15.0, 1%, 0.1 W, 0603	0603	CRCW060315R0FKEA	Vishay-Dale		

Table 4. Bill of Materials (continued)

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
R712_7, R713_7, R714_7, R715_7, R716_7, R717_7, R812_8, R813_8, R814_8, R815_8, R816_8, R817_8	12	0	RES, 0, JUMPER, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic		
R718_7, R719_7, R818_8, R819_8	4	24.9	RES, 24.9, 1%, 0.1 W, 0603	0603	CRCW060324R9FKEA	Vishay-Dale		
R802_8	1	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	CRCW040249R9FKED	Vishay-Dale		
R804_8, R805_8	2	64.9	RES, 64.9, 1%, 0.063 W, 0402	0402	CRCW040264R9FKED	Vishay-Dale		
R806_8, R807_8	2	169	RES, 169, 1%, 0.063 W, 0402	0402	CRCW0402169RFKED	Vishay-Dale		
R808_8, R809_8	2	348	RES, 348, 1%, 0.063 W, 0402	0402	CRCW0402348RFKED	Vishay-Dale		
SHUNT_JP2, SHUNT_JP3, SHUNT_JP4, SHUNT_JP5, SHUNT_JP6, SHUNT_JP7, SHUNT_JP8, SHUNT_JP9, SHUNT_JP10, SHUNT_JP11, SHUNT_JP12, SHUNT_JP13, SHUNT_JP28, SHUNT_JP33, SHUNT_JP88_1, SHUNT_JP88_2, SHUNT_JP89_1, SHUNT_JP89_2, SHUNT_JP506_1, SHUNT_JP506_2, SHUNT_JP700_7, SHUNT_JP800_8	22			MJ-5.97-G OR EQUIVALENT		KELTRON		
SW1	1	12 V	SWITCH, TACTILE SPST-NO, 0.05A, 12 VDC, TH-2 PIN	-	PTS635SL43LFS	C&K COMPONENTS	-	-
SW2, SW3	2		Switch, Push Button, SMD	2.9x2x3.9mm SMD	SKRKAAE010	Alps	Equivalent	Any
T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T24	24		TRANSFORMER, RF, 50 OHM, 0.03 TO 125 MHZ, 6-PIN, SMT, ROHS	-	ADT1-6T	MINI-CIRCUITS	-	-
TADC_CLK, TSYSREF	2		TRANSFORMER, RF, 50 OHM, 2 MHZ TO 755 MHZ, 6-PIN, ROHS	-	ADT4-1WT	MINI-CIRCUITS	-	-
TP1, TP2, TP3, TP8, TP9, TP10, TP11, TP13, TP15, TP19, TP20, TP23, TP24, TP35, TP36, TP37, TP38, TP111, TPA0, TPA1, TPA2, TPA3, TPA4, TPA5, TPA6, TPA7, TPB0, TPB1, TPB2, TPB3, TPB4, TPB5	32	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
TP4, TP5, TP6, TP7, TP21, TP22, TP25, TP26	8	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		
TP12, TP14, TP17, TP18, TP141	5	Blue	Test Point, Miniature, Blue, TH	Blue Miniature Testpoint	5117	Keystone		
U1	1		BGA-198, MULTI-CHANNEL HIGH SPEED ADC WITH JESD204B INTERFACE	-	ADS52J90ZZE	TEXAS INSTRUMENTS	-	-
U2	1			NKD0064A	LMK04826BISQ/NOPB	Texas Instruments		None
U4	1		IC, INVERT SCHMITT-TRIG, SC70-5	DCK	SN74AUP1T14DCK	TEXAS INSTRUMENTS	-	-
U5	1		IC, REG LDO, 3.3V, 0.1A, SOT23-5	DBV	TPS76933DBV	TEXAS INSTRUMENTS	-	-

Table 4. Bill of Materials (continued)

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
U6	1		Quad High Speed USB to Multipurpose UART/MPSSE IC	LQFP_10x10mm	FT4232HL	FTDI		
U7	1		IC, EEPROM, 1KBIT, 2MHZ, 8-SOIC	SN	93LC46BT-I/SN	MICROCHIP TECHNOLOGY	-	-
U8, U11, U13	3		IC, REG LDO, ADJ, 1A, 20-VQFN	RGW	TPS7A4700RGW	TEXAS INSTRUMENTS	-	-
U9	1		IC, OVERVOLT PROT CTRLRL, SOT23-5	DBV	TPS2400DBV	TEXAS INSTRUMENTS	-	-
U10	1		IC, ULTRALOW-NOISE, HIGH PSRR, FAST, RF, 1A LOW-DROPOUT LINEAR REGULATORS, SOT223-6	DCQ	TPS79601DCQ	TEXAS INSTRUMENTS	-	-
U12	1		IC, REG, BUCK, SYNC, ADJ, 3A, 16-WQFN	RTE	TPS54319RTE	TEXAS INSTRUMENTS	-	-
U14	1		IC, BUS, TXRX, TRI-ST, 2BIT, SM-8	DCT	SN74AVC2T45DCT	TEXAS INSTRUMENTS	-	-
U15	1		150 Mbps Quad Channels, 3 / 1, Digital Isolator, -40 to +125 degC, 16-pin SOIC (DW), Green (RoHS & no Sb/Br)	DW0016A	ISO7241MDW	TEXAS INSTRUMENTS	Equivalent	None
U16, U18	2		IC, 4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS, TSSOP-16	PW	SN74AVC4T245PW	TEXAS INSTRUMENTS	-	-
U17	1		150 Mbps Quad Channels, 4 / 0, Digital Isolator, 3.3 V / 5 V, -40 to +125 degC, 16-pin SOIC (DW), Green (RoHS & no Sb/Br)	DW0016A	ISO7240MDW	Texas Instruments	Equivalent	None
U800_8	1		IC, WIDEBAND, LOW-NOISE, LOW-DISTORTION, FULLY-DIFFERENTIAL AMPLIFIER, 16-QFN	RGT	THS4509RGT	TEXAS INSTRUMENTS		
XTAL1	1	10 MHZ	OSCC, HCMOS, 3.3 V, +/-25 PPM, 10 MHZ, SMT, 6P	-	FXO-HC736R-10	FOX	-	-
XTAL2	1		OSC, 3.3 V, 40 MHz, SMD	SMD, 4-Leads, Body 7x5mm	FXO-HC735-40	Fox Electronics		
Y3	1		CRYSTAL 12.000MHZ 10PF SMD	3.2x0.55x2.5mm	ABM8G-12.000MHZ-B4Y-T	Abracor Corporation		
Z_SCREW1, Z_SCREW2, Z_SCREW3, Z_SCREW4, Z_SCREW5	5				PMSSS 440 0075 PH	BUILDING FASTENERS		
C13, C14, C15, C16, C17	0	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata		
C27, C29, C36, C37, C283, C284, C287, C288	0	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata		
C59, C60	0	22pF	CAP, CERM, 22pF, 100V, +/-5%, COG/NP0, 0603	0603	GRM1885C2A220JA01D	MuRata		
C71, C91, C95, C113	0	4.7uF	CAP, TANTALUM, 4.7uF, 10%, 10V, SMT3528-21	3528-21	TAJB475K010RNJ	AVX	-	-
C108	0	3300pF	CAP, CERAMIC, 3300pF, 50V, 10%, X7R, 0603	0603	06035C332KAT2A	AVX	-	-
C125, C126, C135, C136, C145, C146, C155, C156, C165, C166, C175, C176, C185, C186, C195, C196, C205, C206, C215, C216, C225, C226, C235, C236	0	0.1uF	CAP, CERAMIC, 0.1uF, 16V, 10%, X7R, 0402	0402	0402YC104KAT2A	AVX	-	-
C705_7, C805_8	0	0.1uF	CAP, CERM, 0.1 μF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX		
C708_7, C709_7, C710_7, C711_7, C808_8, C809_8, C810_8, C811_8	0	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, COG/NP0, 0603	0603	C1608C0G2A102J	TDK		
C801a_8	0	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	0603	GRM188R71C104KA01D	MuRata		
F1	0		FUSE 2.0A 63V FAST	1206	1206SFF200F/63-2	TE Connectivity		

Table 4. Bill of Materials (continued)

Reference Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Supplier 1
J35, J36, J37, J38	0		Connector, TH, SMA	SMA	142-0701-201	Emerson Network Power		
JP15, JP16	0		CONN, HEADER, 2POS, .100", T/H GOLD	-	HTSW-102-08-G-S	SAMTEC	-	-
L700_7, L701_7, L702_7, L703_7, L800_8, L801_8, L802_8, L803_8	0	60nH	Inductor, Multilayer, 60nH, 3.37 A, 0.0219 ohm, SMD	0603	MDT1608-CLHR06	Toko		
R1, R2, R5, R6, R9, R10	0	169	RES, 169 ohm, 1%, 0.063W, 0402	0402	CRCW0402169RFKED	Vishay-Dale		
R3, R4, R7, R8, R11, R12	0	49.9	RES, 49.9 ohm, 1%, 0.063W, 0402	0402	CRCW040249R9FKED	Vishay-Dale		
R19, R20, R23, R24, R35, R36, R41, R42, R47, R48	0	240 OHM	RESISTOR, THICK FILM, 240 OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF2400X	PANASONIC	-	-
R62, R94, R99, R101, R113, R114, R121, R122, R127, R128, R134, R136, R141, R142, R149, R150, R155, R156, R163, R164, R169, R170, R176, R178, R183, R184, R191, R192, R197, R198, R204, R206, R211, R213, R218, R220, R225, R226, R233, R234, R239, R240, R247, R248, R253, R254, R261, R262, R267, R268, R275, R276, R594	0	0	RESISTOR, THICK FILM, 0 OHM, JUMPER, 0.1W, SMT0402	0402	ERJ-2GE0R00X	PANASONIC		
R97, R100	0	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	ERJ-3GEY0R00V	Panasonic		
R108	0	10K OHM	RESISTOR, THICK FILM, 10K OHM, 1%, 0.1W, SMT0603	0603	ERJ-3EKF1002V	PANASONIC	-	-
R109	0	10.0	RES, 10.0 ohm, 1%, 0.063W, 0402	0402	CRCW040210R0FKED	Vishay-Dale		
R117, R118, R131, R132, R145, R146, R159, R160, R173, R174, R187, R188, R201, R202, R215, R216, R229, R230, R243, R244, R257, R258, R271, R272	0	49.9	RESISTOR, THICK FILM, 49.9 OHM, 1%, 0.1W, SMT0402	0402	ERJ-2RKF49R9X	PANASONIC	-	-
R673, R674, R678, R679	0	0	RESISTOR, THICK FILM, 0 OHM, JUMPER, 0.063W, SMT0402	0402	CRCW04020000Z0ED	VISHAY	-	-
R700_7, R701_7, R800_8, R801_8	0	249	RES, 249, 1%, 0.063 W, 0402	0402	CRCW0402249RFKED	Vishay-Dale		
R702_7	0	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	CRCW040249R9FKED	Vishay-Dale		
R704_7, R705_7	0	64.9	RES, 64.9, 1%, 0.063 W, 0402	0402	CRCW040264R9FKED	Vishay-Dale		
R720_7, R721_7, R820_8, R821_8	0	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	CRCW060349R9FKEA	Vishay-Dale		
R724_7, R725_7, R726_7, R727_7	0	0	RES, 0, 1%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America		
TP16	0	Blue	Test Point, Miniature, Blue, TH	Blue Miniature Testpoint	5117	Keystone		
U700_7	0		IC,WIDEBAND, LOW-NOISE, LOW-DISTORTION, FULLY-DIFFERENTIAL AMPLIFIER, 16-QFN	RGT	THS4509RGT	TEXAS INSTRUMENTS		
Notes:	d in the Alternate PartNumber and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.							

5.2 Schematics

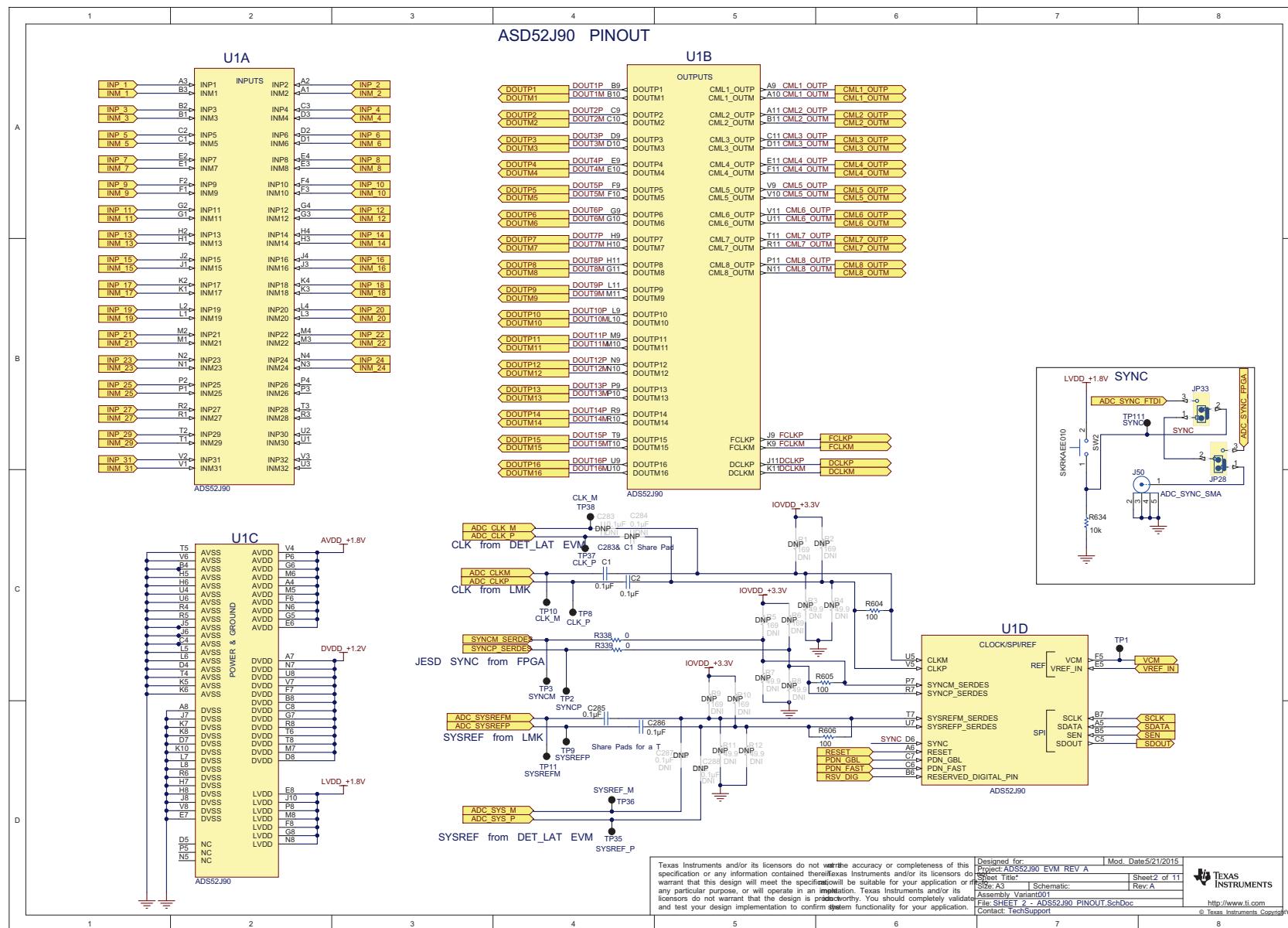
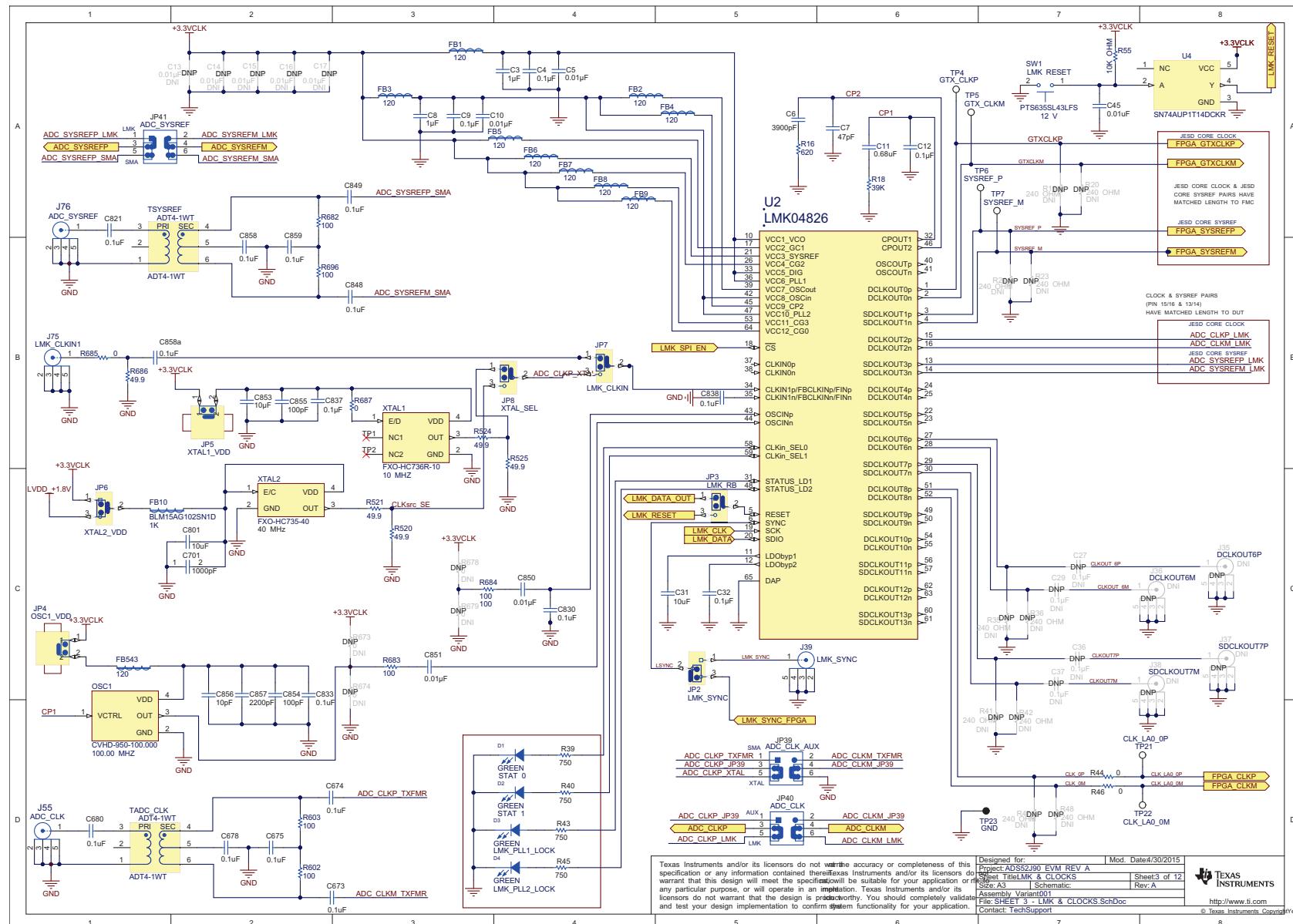


Figure 28. ADS52J90 EVM Schematic (Page 1)


Figure 29. ADS52J90 EVM Schematic (Page 2)

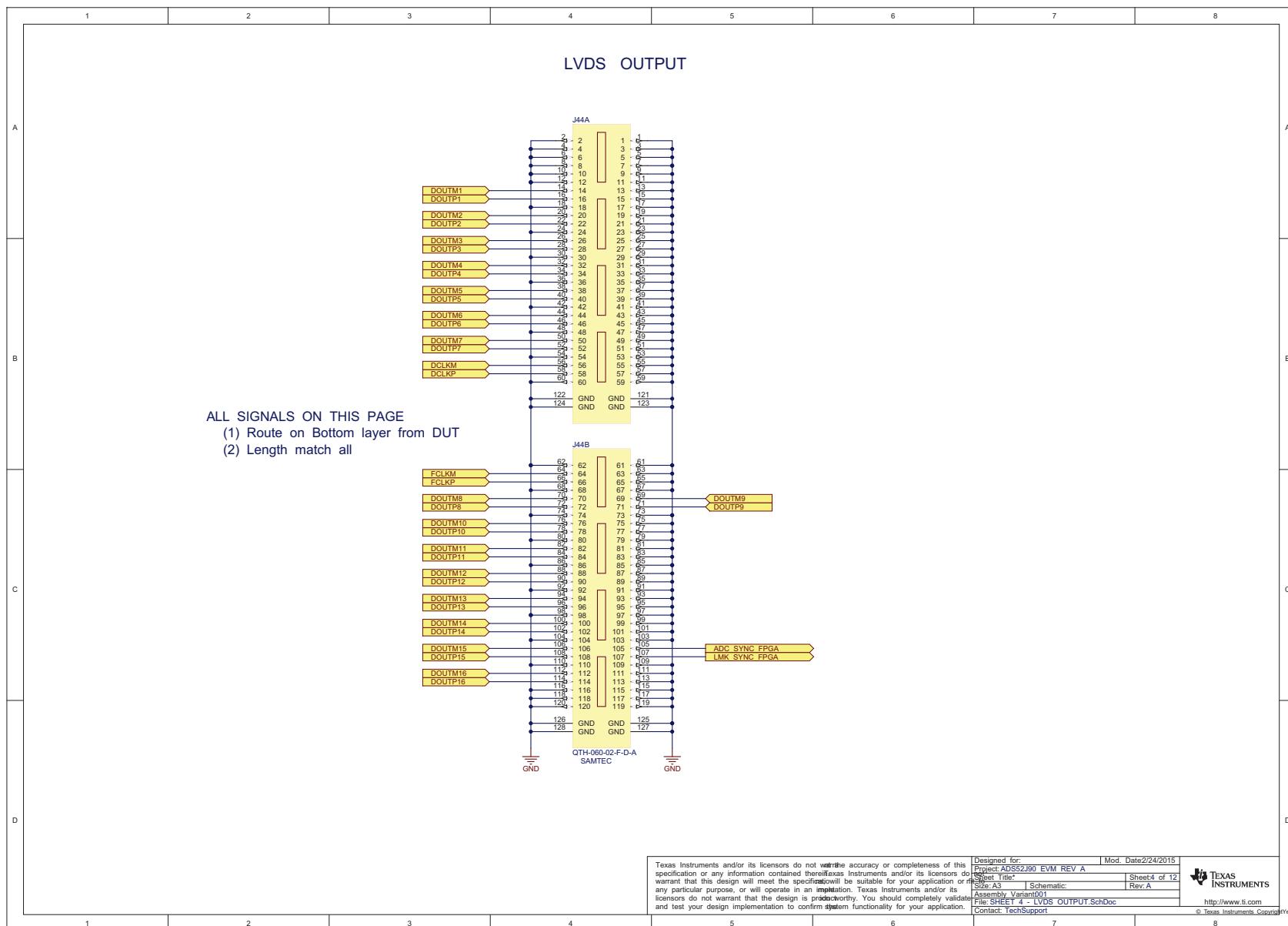


Figure 30. ADS52J90 EVM Schematic (Page 3)

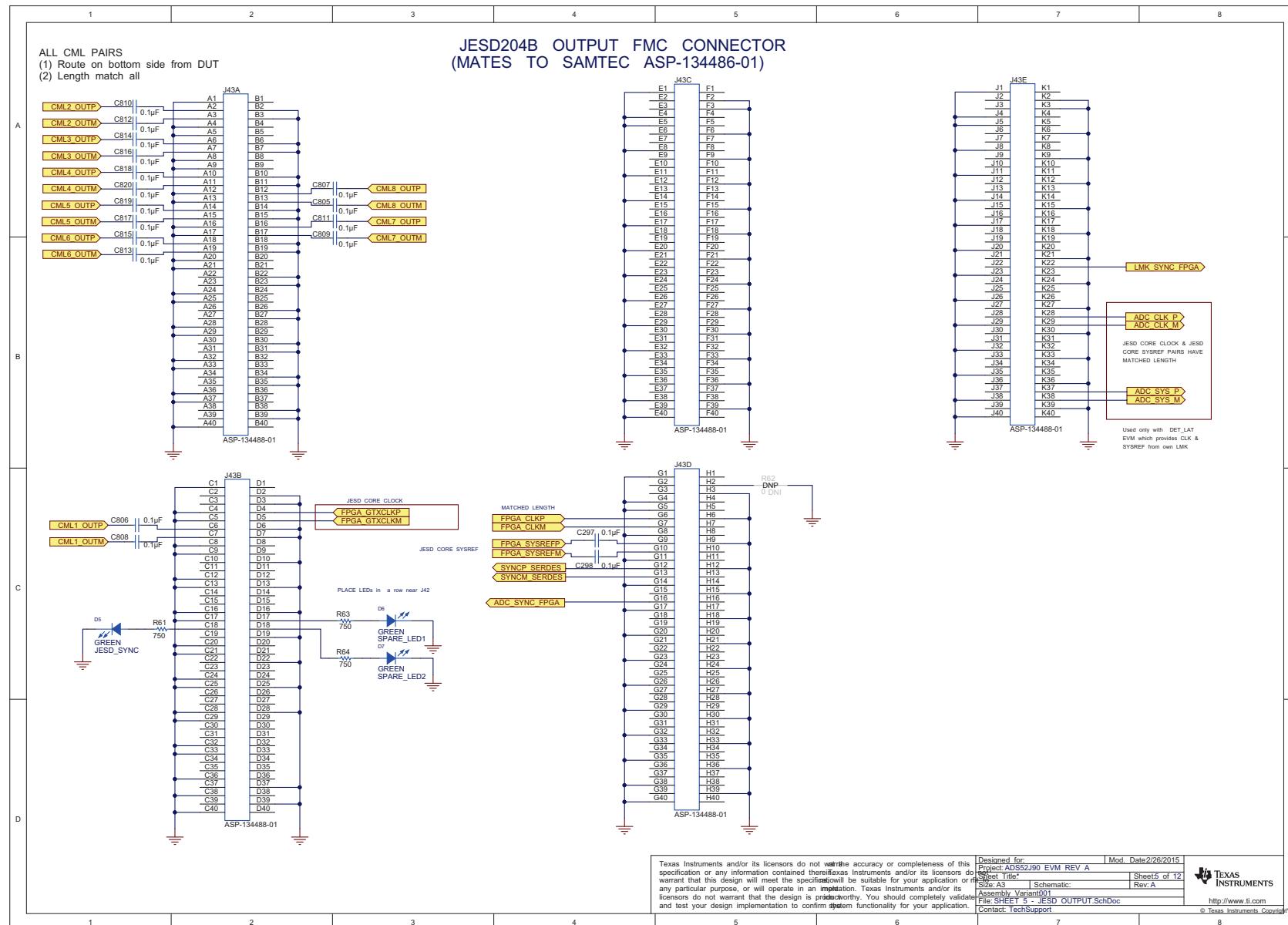


Figure 31. ADS52J90 EVM Schematic (Page 4)

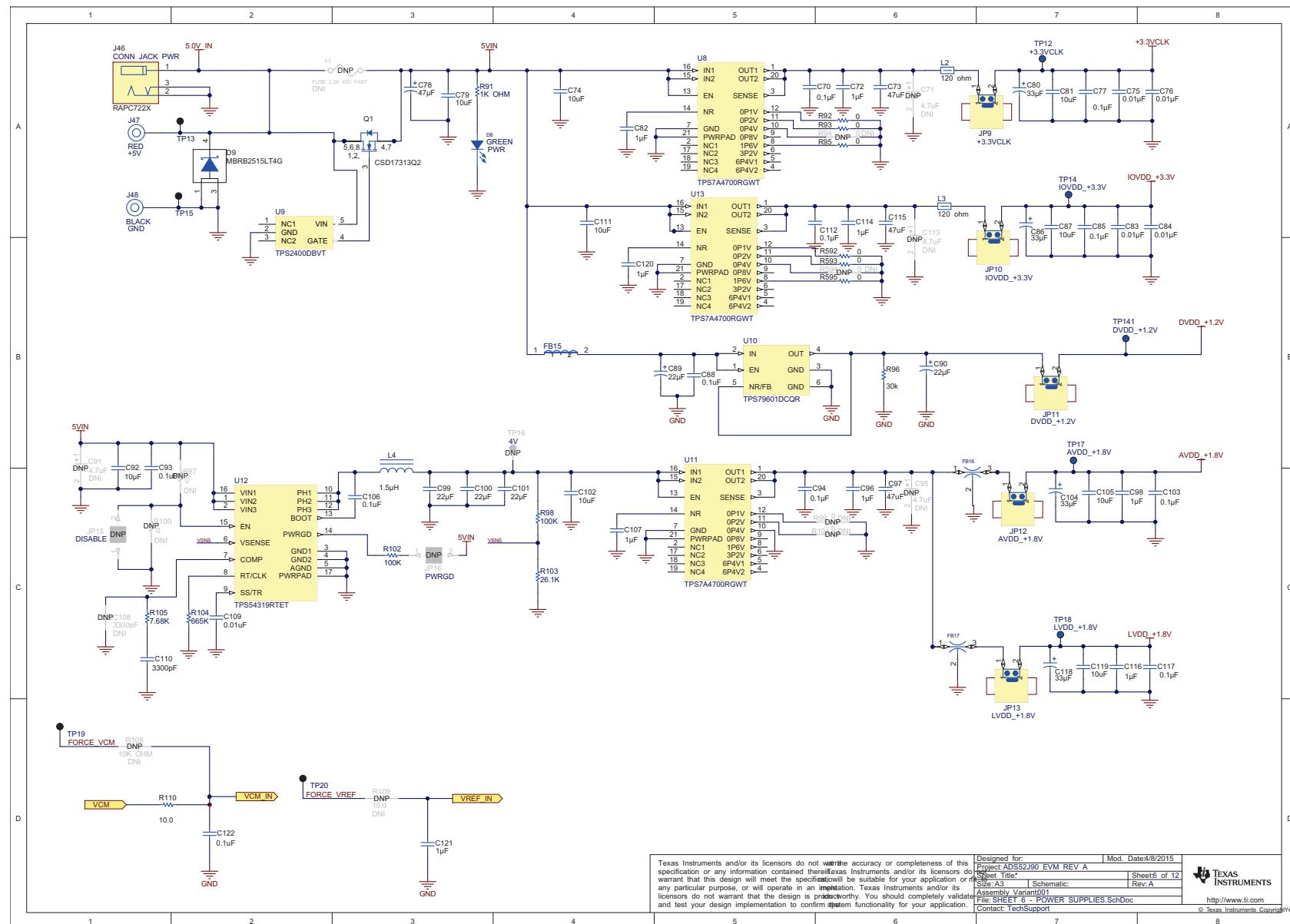
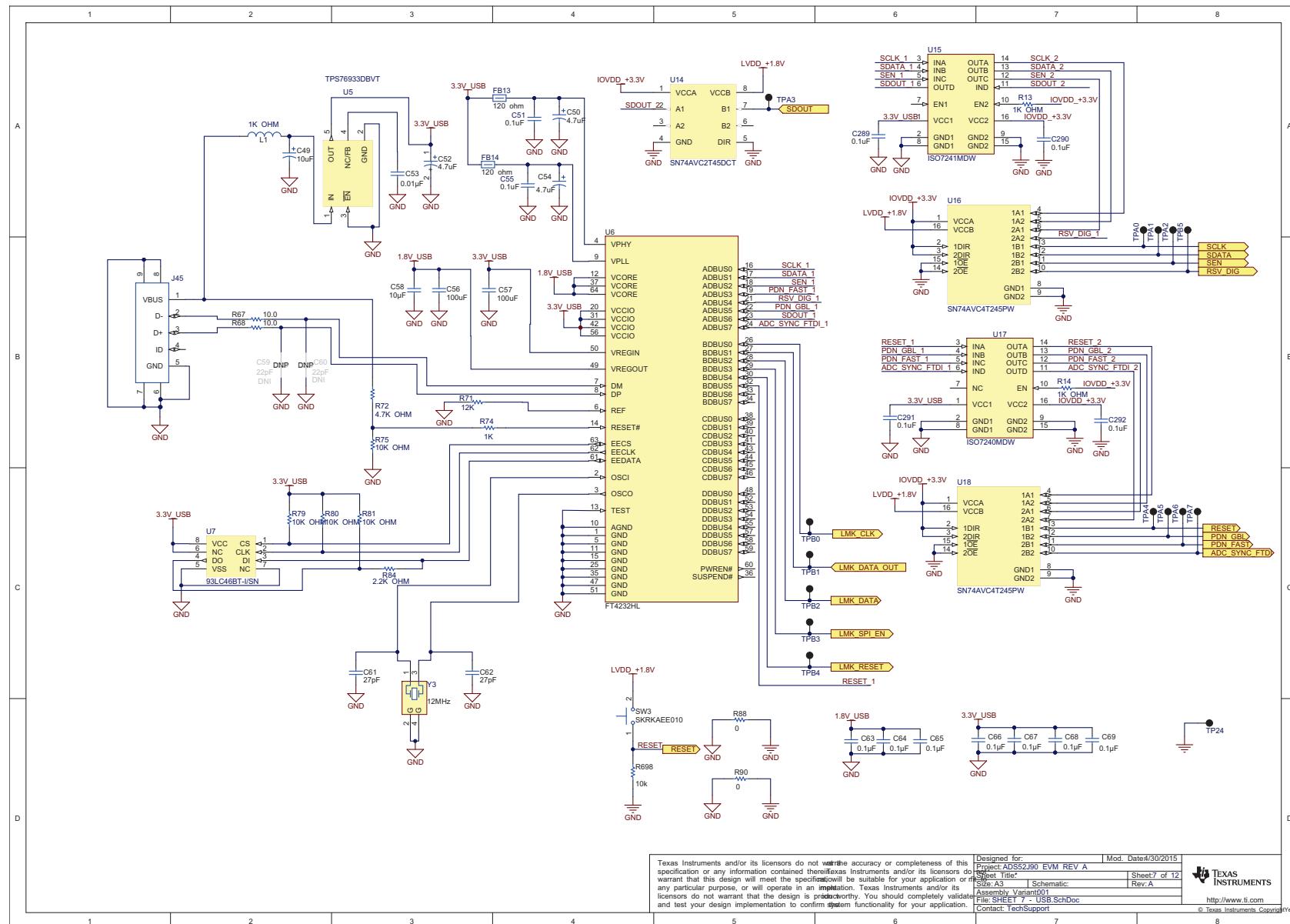


Figure 32. ADS52J90 EVM Schematic (Page 5)


Figure 33. ADS52J90 EVM Schematic (Page 6)

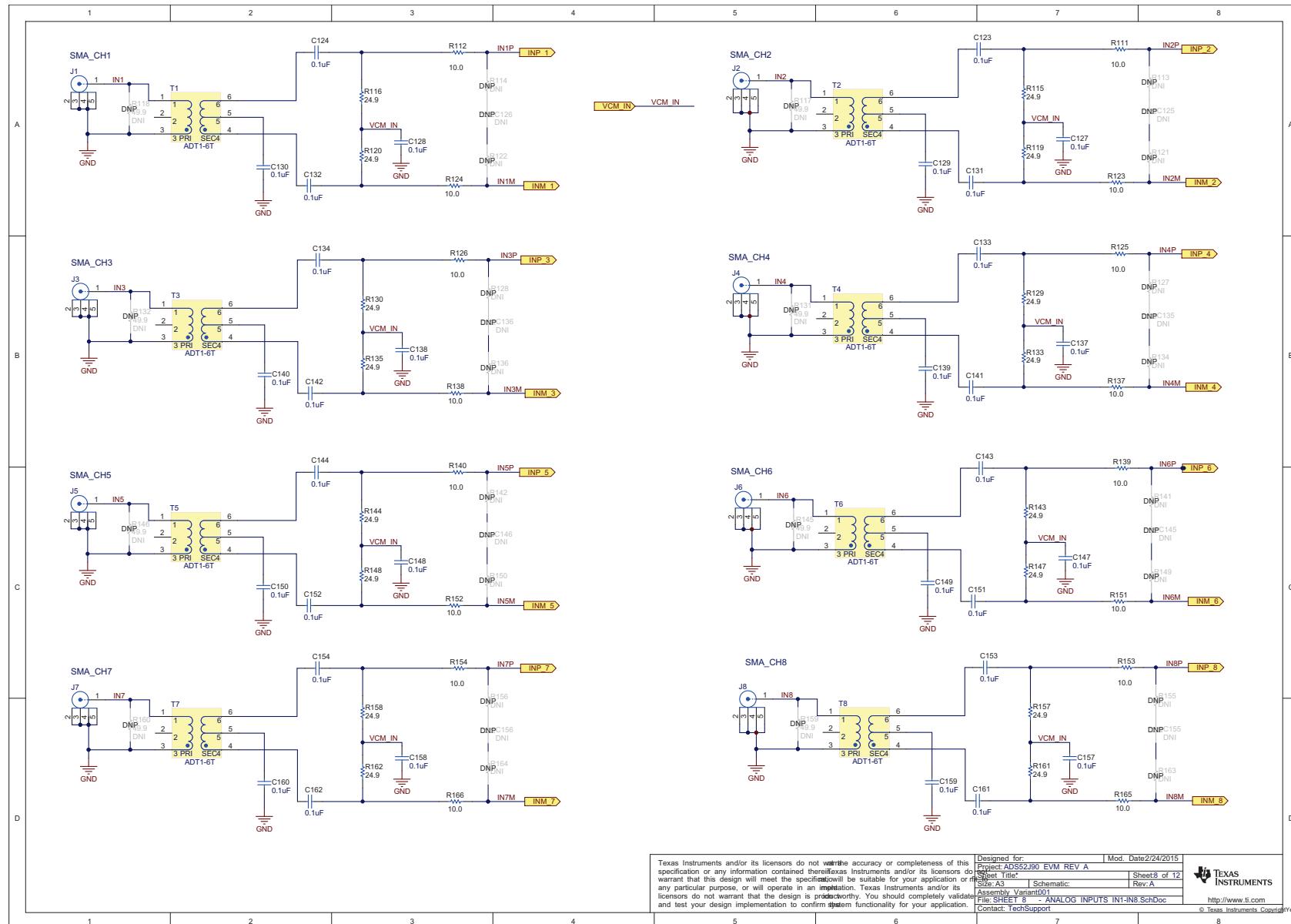
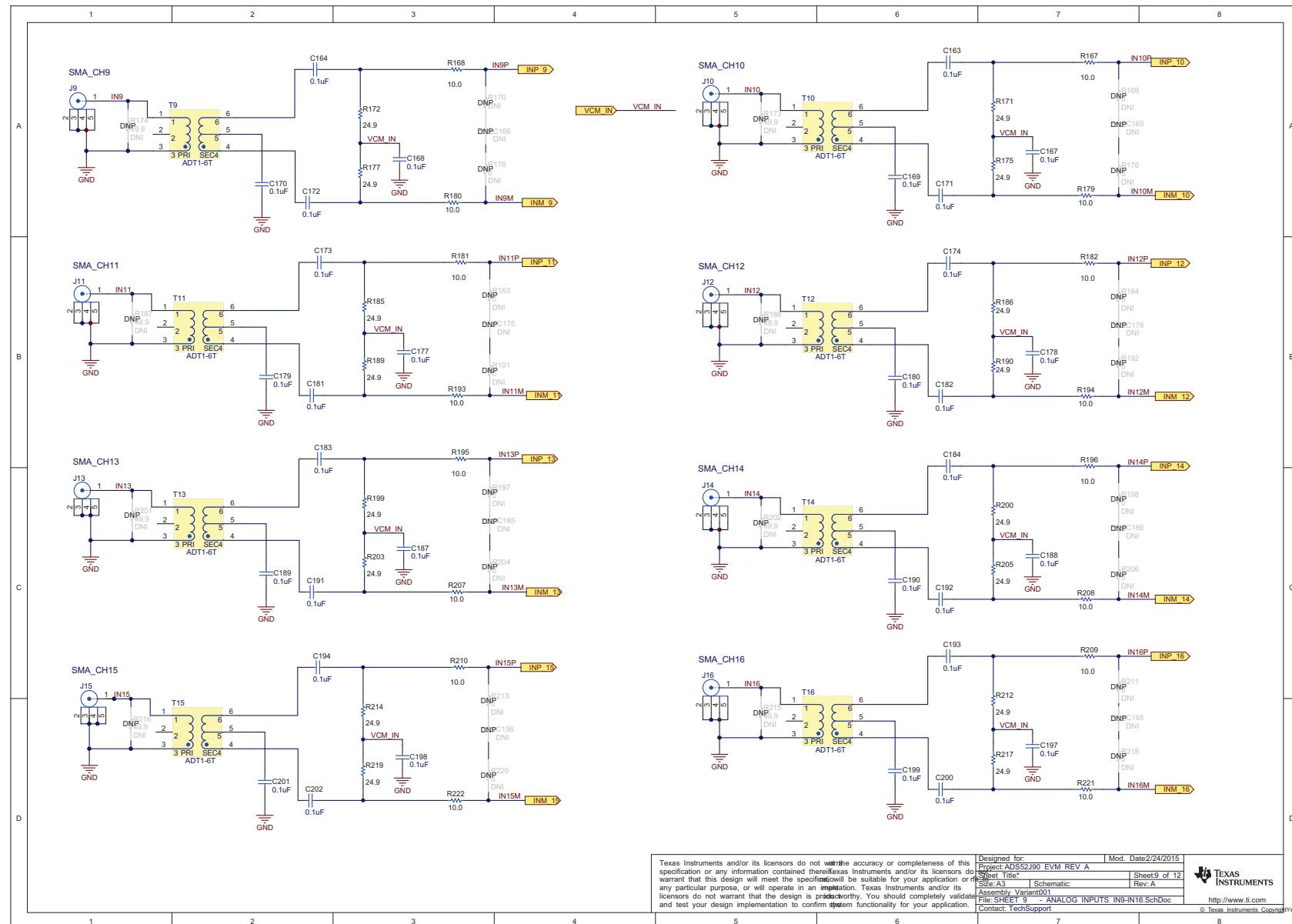


Figure 34. ADS52J90 EVM Schematic (Page 7)


Figure 35. ADS52J90 EVM Schematic (Page 8)

Designed for:	Mod. Date 2/24/2015
Project:	ADS52J90 EVM REV A
Spec Title*:	Sheet 9 of 12
Rev. A:	Schematic: Rev. A
Assembly Variant 001:	
File:	SHEET 9 - ANALOG INPUTS IN9-IN16.SchDoc
Contact:	TechSupport
© Texas Instruments Copying Year:	

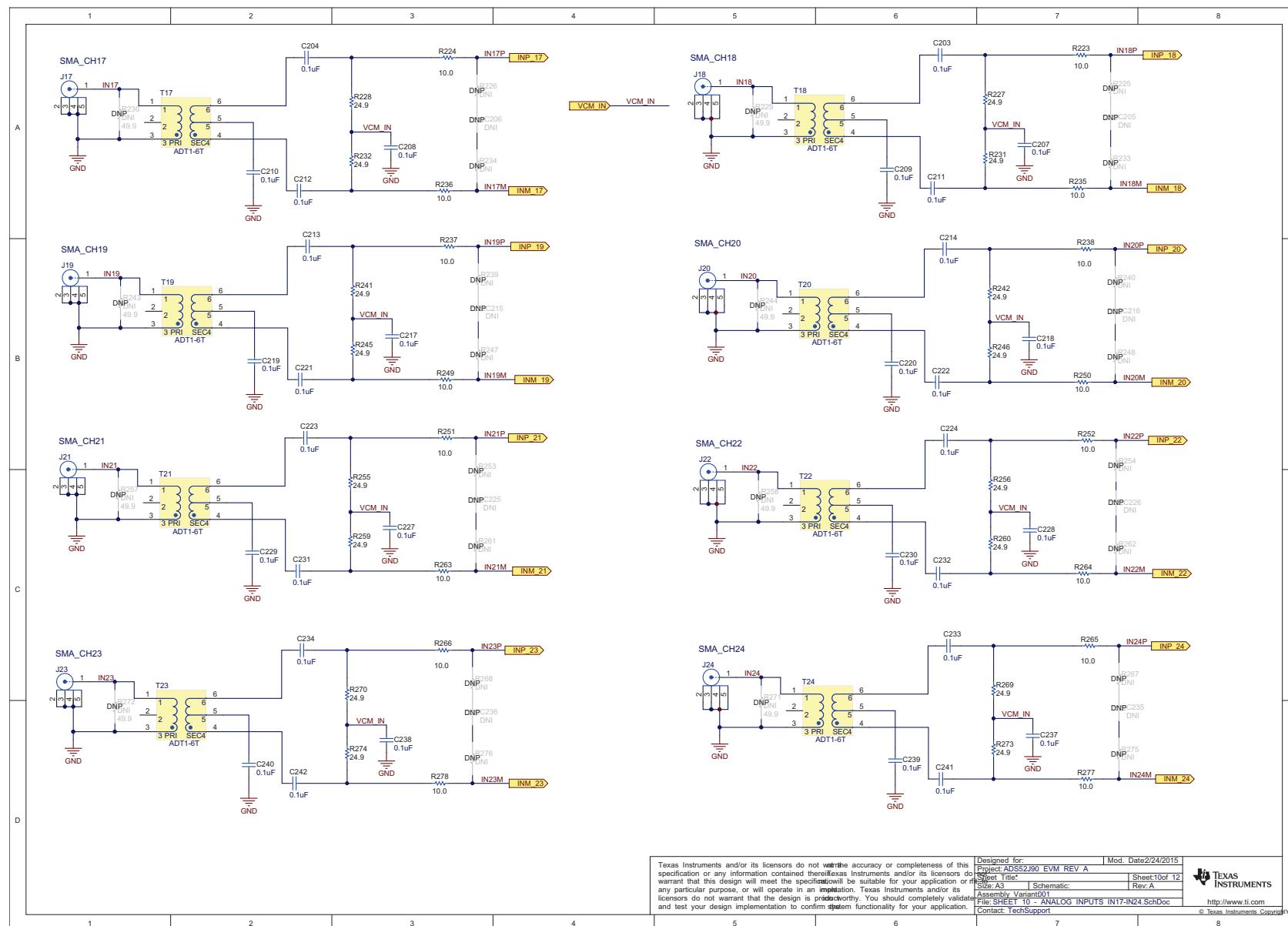
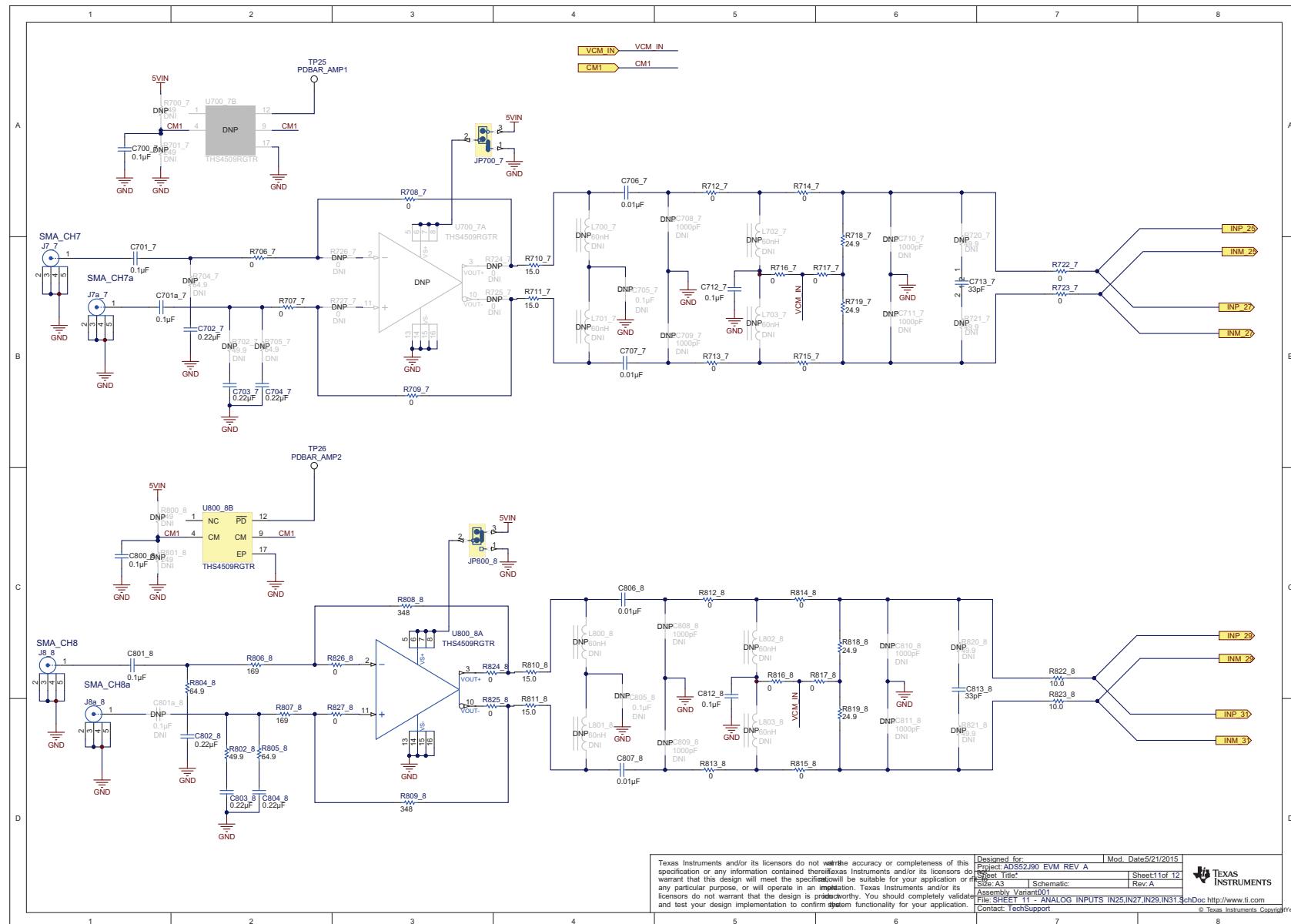
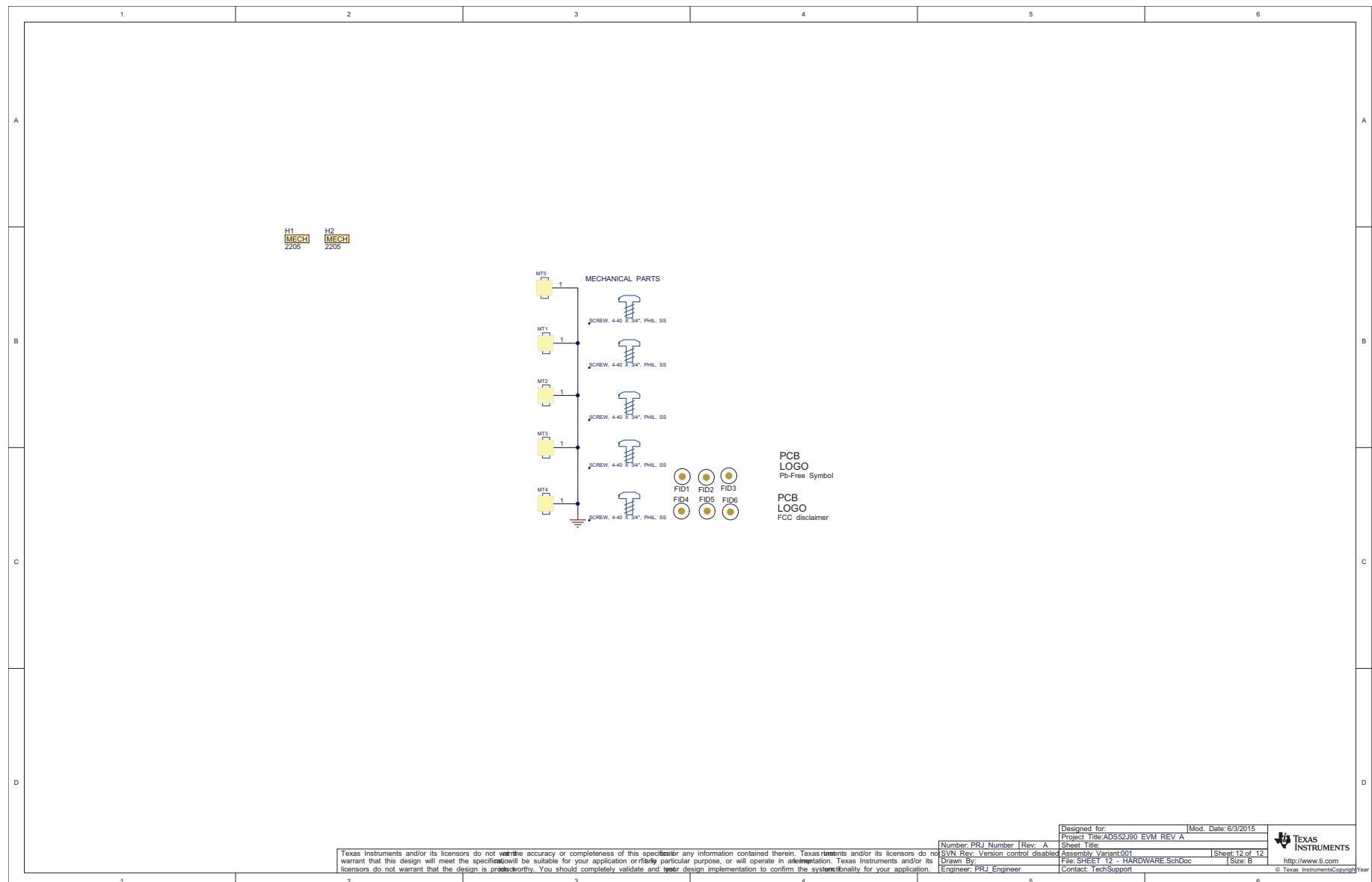


Figure 36. ADS52J90 EVM Schematic (Page 9)


Figure 37. ADS52J90 EVM Schematic (Page 10)


Figure 38. ADS52J90 EVM Schematic (Page 11)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (June 2016) to B Revision

Page

- | | |
|--|---|
| • Added note about REACH compliance..... | 1 |
| • Added Table 1: List of SVHCs..... | 1 |

Changes from Original (October 2015) to A Revision	Page
• Added Section 5	27

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