LM78L 100mA Fixed Output Linear Regulator

1 Features

- Input voltage: up to 30V operating
  - 45V absolute maximum (new chip)
- Available output voltages:
  - Legacy chip: 5V, 6.2V, 8.2V, 9V, 12V, 15V
  - New chip: 3.3V, 5V, 6V, 12V, 15V
- Output current: 100mA
- Internal thermal overload protection
- Output current limiting
- No external components required for stability
- Package options:
  - Legacy chip: SOIC-8, TO-92-3, DSBGA-8
  - New chip: SOIC-8, SOT-89-3

2 Applications

- Servo & stepper drives
- Battery chargers
- Portable instrumentation
- LED lighting
- Appliances

3 Description

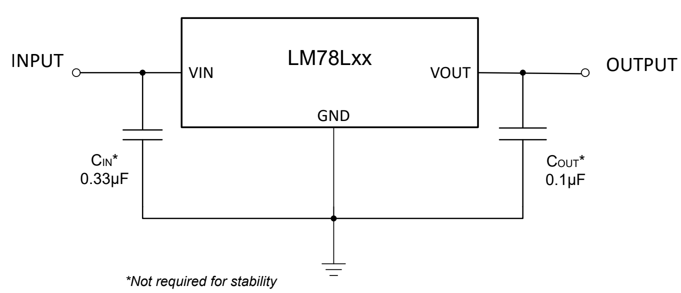
The LM78L series (LM78Lxx throughout this document) of positive linear regulators is available with several fixed output voltages, making the devices useful in a wide range of applications. Used as a Zener-diode and resistor combination replacement, the LM78Lxx typically provides an effective output impedance improvement of two orders of magnitude and lower quiescent current. These regulators can provide local, on-card regulation, eliminating distribution problems associated with single-point regulation. The available voltages allow the LM78Lxx to be used in logic systems, instrumentation, HiFi, and other solid-state electronic equipment.

The LM78Lxx with new chip is available in SOIC (D) package and SOT-89 (PK) packages. The LM78Lxx series regulators can deliver up to 100mA output current. Current limiting is included to limit the peak output current to a safe value. If internal power dissipation is too high, the thermal shutdown circuit prevents the IC from overheating.

Table 3-1. Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(3)
LM78L	D (SOIC, 8)	4.90mm × 6.00mm
	PK (SOT-89, 3)(2)	4.50mm × 4.095mm
	LP (TO-92, 3)	5.20mm × 3.68mm
	YPB (DSBGA, 8)	1.30mm × 1.30mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) Preview Only
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Fixed Output Regulator Circuit

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4 Pin Configuration and Functions

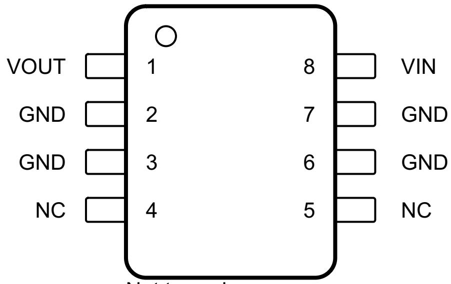


Figure 4-1. D Package 8-Pin SOIC Top View

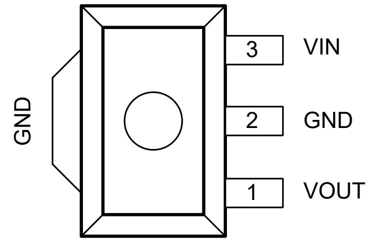


Figure 4-2. PK Package 3-Pin SOT-89 Top View

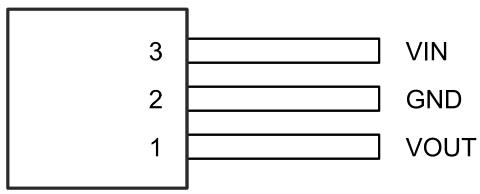


Figure 4-3. LP Package 3-Pin TO-92 Bottom View

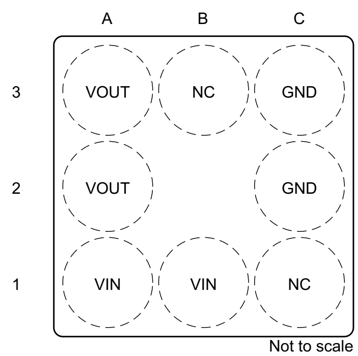


Figure 4-4. YPB Package 8-Pin DSBGA Top View

Table 4-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	SOIC	SOT-89	TO-92	DSBGA		
GND	2, 3, 6, 7	2	2	C2, C3	—	Ground
NC	4, 5	—	—	B3, C1	—	No connection
VIN	8	3	3	A1, B1	I	Input supply voltage pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the VIN and GND pins of the device as possible.
VOUT	1	1	1	A2, A3	O	Output voltage pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the VOUT and GND pins of the device as possible.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage, V_{IN} (legacy chip)			35	V
Input voltage, V_{IN} (new chip)			45	V
Operating junction temperature, T_J (legacy chip)	LM78LxxACZ (TO-92)	0	125	°C
	LM78LxxACM (SOIC)	0	125	
	LM78LxxAIM (SOIC)	-40	125	
	LM78LxxITP (thin DSBGA)	-40	85	
Operating junction temperature, T_J (new chip)		-40	150	°C
Storage temperature, T_{stg} (legacy and new chip)		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1000	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	-	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		LM78Lxx					UNIT
		D (SOIC) - New Chip	D (SOIC) - Legacy Chip	PK (SOT-89)	LP (TO-92)	YPB (DSBGA)	
		8 PINS	8 PINS	3 PINS	3 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	128.8	54.7	158.7	108.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	76	88.1	75.2	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	69.3	9.6	—	31.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.2	26.3	6.2	30.2	4.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55	68.8	9.7	138.2	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	7.7	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage (legacy chip)			30	V
	Input voltage (new chip)	5.3		30	
I_O	Continuous output current (legacy and new chip)			100	mA
C_{IN} [2]	Input capacitor [3] (new chip only)		0.33		µF
C_{OUT} [2]	Output capacitor [4] (new chip only)		0.1		

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	TYP	MAX	UNIT
T_J	Operating junction temperature (legacy chip)	LM78LxxACZ (TO-92)	0		125	°C
		LM78LxxACM (SOIC)	0		125	
		LM78LxxAIM (SOIC)	-40		125	
		LM78LxxITP (DSBGA)	-40		85	
	Operating junction temperature (new chip)		-40		125	°C

(1) All voltages are with respect to GND.
(2) LM78Lxx does not require any external capacitors for LDO stability.
(3) An input capacitor with value of 0.33µF is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(4) An output capacitor with value of 0.1µF is recommended to improve the load and line transient performance of the LM78Lxx regulator.

5.5 Electrical Characteristics: LM78L33 (New Chip Only)

at specified junction temperature, V_{IN} = 9V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_O	Output voltage	V_{IN} = 5.5V to 20V, and I_O = 1mA to 40mA	T_J = 25°C	3.26	3.3	3.44	V
		V_{IN} = 5.5V to 20V, and I_O = 1mA to 40mA	T_J = full range	3.21		3.47	
		I_O = 1mA to 70mA		3.23		3.45	
V_O	Output voltage	V_{IN} = 5.5V to 20V, and I_O = 1mA to 40mA	T_J = -40°C to 140°C	3.21		3.47	V
		I_O = 1mA to 70mA		3.21		3.45	
ΔV_O	Line regulation	V_{IN} = 5.5V to 20V	T_J = 25°C		36	60	mV
		V_{IN} = 6V to 20V			24	40	
	Load regulation	I_O = 1mA to 100mA	T_J = 25°C		25	30	mV
		I_O = 1mA to 40mA			10	15	
I_Q	Quiescent current	T_J = 25°C			3.8	5	mA
		T_J = 125°C				5.5	
ΔI_Q	Quiescent current change	V_{IN} = 6V to 20V	T_J = full range			1.4	mA
		I_O = 1mA to 40mA				0.01	
V_n	Output noise voltage	f = 10Hz to 100kHz	T_J = 25°C		85		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120Hz, V_{IN} = 6V to 20V	T_J = 25°C	49	57.5		dB
I_{PK}	Peak output current	T_J = 25°C			210		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5mA	T_J = 25°C		0.07		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	ΔV_O = 2% of V_O	T_J = 25°C		5	5.3	V

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. Refer to the *Recommended Operating Conditions* table for the operating temperature ranges of each package.

5.6 Electrical Characteristics: LM78L05 (Legacy and New Chip)

at specified junction temperature, V_{IN} = 10V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
V_O	Output voltage	Legacy chip	T_J = 25°C		4.8	5	5.2	V
			V_{IN} = 7V to 20V, and I_O = 1mA to 40mA[2]	T_J = full range	4.75		5.25	
			I_O = 1mA to 70mA[2]		4.75		5.25	
		New chip	T_J = 25°C		4.8	5	5.2	
			V_{IN} = 7V to 20V, and I_O = 1mA to 40mA	T_J = full range	4.75		5.25	
			I_O = 1mA to 70mA		4.85		5.15	

at specified junction temperature, V_{IN} = 10V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
V_O	Output voltage	New chip	V_{IN} = 7V to 20V, and I_O = 1mA to 40mA	T_J = -40 to 140°C	4.75		5.25	V
			I_O = 1mA to 70mA		4.85		5.15	
ΔV_O	Line regulation	Legacy chip	V_{IN} = 7V to 20V	T_J = 25°C		18	75	mV
			V_{IN} = 8V to 20V			10	54	
		New chip	V_{IN} = 7V to 20V			32	75	
			V_{IN} = 8V to 20V			26	54	
	Load regulation	Legacy chip	I_O = 1mA to 100mA	T_J = 25°C		20	60	mV
			I_O = 1mA to 40mA			5	30	
		New chip	I_O = 1mA to 100mA			22	60	
			I_O = 1mA to 40mA			10	30	
I_Q	Quiescent current	Legacy chip	T_J = 25°C			3	5	mA
		New chip	T_J = 25°C			3.8	5	
			T_J = 125°C				5.5	
ΔI_Q	Quiescent current change	Legacy chip	V_{IN} = 8V to 20V	T_J = full range			1	mA
			I_O = 1mA to 40mA				0.1	
		New chip	V_{IN} = 8V to 20V				1	
			I_O = 1mA to 40mA				0.01	
V_n	Output noise voltage	Legacy chip[3]	f = 10Hz to 100kHz	T_J = 25°C		40		µV
		New chip				125		
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	Legacy chip	f = 120Hz, V_{IN} = 8V to 16V	T_J = 25°C	47	62		dB
		New chip	f = 120Hz, V_{IN} = 8V to 16V		47	49		
I_{PK}	Peak output current	Legacy chip	T_J = 25°C			140		mA
		New chip	T_J = 25°C			210		
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	Legacy chip	I_O = 5mA	T_J = 25°C		–0.65		mV/°C
		New chip	I_O = 5mA	T_J = 25°C		0.044		
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	Legacy chip	ΔV_O = 2% of V_O	T_J = 25°C		6.7	7	V
		New chip	ΔV_O = 2% of V_O	T_J = 25°C		6.7	7	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. Refer to the *Recommended Operating Conditions* table for the operating temperature ranges of legacy and new chip.
(2) Power dissipation ≤ 0.75W.
(3) Recommended minimum load capacitance of 0.01µF to limit high-frequency noise.

5.7 Electrical Characteristics: LM78L06 (New Chip Only)

at specified junction temperature, V_{IN} = 12V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_O	Output voltage	V_{IN} = 8.5V to 20V, and I_O = 1mA to 40mA	T_J = 25°C	5.82	6	6.19	V
		V_{IN} = 8.5V to 20V, and I_O = 1mA to 40mA	T_J = full range	5.76		6.24	
		I_O = 1mA to 70mA		5.76		6.24	
V_O	Output voltage	V_{IN} = 8.5V to 20V, and I_O = 1mA to 40mA	T_J = -40°C to 140°C	5.76		6.24	V
		I_O = 1mA to 70mA		5.76		6.24	
ΔV_O	Line regulation	V_{IN} = 8.5V to 20V	T_J = 25°C		65	175	mV
		V_{IN} = 9V to 20V			55	125	
	Load regulation	I_O = 1mA to 100mA	T_J = 25°C		25	80	mV
		I_O = 1mA to 40mA			10	40	
I_Q	Quiescent current	T_J = 25°C			3.8	5	mA
		T_J = 125°C				5.5	

at specified junction temperature, V_{IN} = 12V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[(1)]		MIN	TYP	MAX	UNIT
ΔI_Q	Quiescent current change	V_{IN} = 8V to 20V	T_J = full range			1.5	mA
		I_O = 1mA to 40mA				0.01	
V_n	Output noise voltage	f = 10Hz to 100kHz	T_J = 25°C		145		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120Hz, V_{IN} = 10V to 20V	T_J = 25°C	40	46		dB
I_{PK}	Peak output current	T_J = 25°C			210		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5mA	T_J = 25°C		-0.088		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	ΔV_O = 2% of V_O	T_J = 25°C		7.7	8	V

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. Refer to the *Recommended Operating Conditions* table for the operating temperature ranges of each package.

5.8 Electrical Characteristics: LM78L09 (Legacy Chip Only)

at specified junction temperature, V_{IN} = 15V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)[(1) (2)]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C		8.64	9	9.36	V
		V_{IN} = 11.5V to 24V, and I_O = 1mA to 40mA[(3)]	T_J = full range	8.55		9.45	
		I_O = 1mA to 70mA[(3)]		8.55		9.45	
ΔV_O	Line regulation	V_{IN} = 11.5V to 24V	T_J = 25°C		100	200	mV
		V_{IN} = 13V to 24V			90	150	
	Load regulation	I_O = 1mA to 100mA	T_J = 25°C		20	90	mV
		I_O = 1mA to 40mA			10	45	
I_Q	Quiescent current	T_J = 25°C			2	5.5	mA
ΔI_Q	Quiescent current change	V_{IN} = 11.5V to 24V	T_J = full range			1.5	mA
		I_O = 1mA to 40mA				0.1	
V_n	Output noise voltage	T_J = 25°C			70		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120Hz, V_{IN} = 15V to 25V	T_J = 25°C	38	44		dB
I_{PK}	Peak output current	T_J = 25°C			140		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5mA	T_J = 25°C		–0.9		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	ΔV_O = 2% of V_O	T_J = 25°C		10.7		V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are verified by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75W.

5.9 Electrical Characteristics: LM78L12 (Legacy and New Chip)

at specified junction temperature, V_{IN} = 19V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[(1)]			MIN	TYP	MAX	UNIT
V_O	Output voltage	Legacy chip	T_J = 25°C		11.5	12	12.5	V
			V_{IN} = 14.5V to 27V, and I_O = 1mA to 40mA[(2)]	T_J = full range	11.4		12.6	
			I_O = 1mA to 70mA[(2)]		11.4		12.6	
		New chip	T_J = 25°C		11.83	12	12.35	
			V_{IN} = 14.5V to 27V, and I_O = 1mA to 40mA	T_J = full range	11.65		12.35	
			I_O = 1mA to 70mA		11.47		12.35	

at specified junction temperature, V_{IN} = 19V, C_{IN} = 0.33μF, C_{OUT} = 0.1μF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
V_O	Output voltage	New chip	V_{IN} = 14.5V to 27V, and I_O = 1mA to 40mA	T_J = -40°C to 140°C	11.65		12.35	V
			I_O = 1mA to 70mA		11.47		12.35	
ΔV_O	Line regulation	Legacy chip	V_{IN} = 14.5V to 27V	T_J = 25°C		30	180	mV
			V_{IN} = 16V to 27V			20	110	
		New chip	V_{IN} = 14.5V to 27V			55	80	
			V_{IN} = 16V to 27V			49	65	
	Load regulation	Legacy chip	I_O = 1mA to 100mA	T_J = 25°C		30	100	mV
			I_O = 1mA to 40mA			10	50	
		New chip	I_O = 1mA to 100mA			33	70	
			I_O = 1mA to 40mA			13	30	
I_Q	Quiescent current	Legacy chip	T_J = 25°C			3	5	mA
		New chip	T_J = 25°C			4	5.1	
			T_J = 125°C				5.5	
ΔI_Q	Quiescent current change	Legacy chip	V_{IN} = 16V to 27V	T_J = full range			1	mA
			I_O = 1mA to 40mA				0.1	
		New chip	V_{IN} = 16V to 27V				0.510	
			I_O = 1mA to 40mA				0.01	
V_n	Output noise voltage	Legacy chip[3]	f = 10Hz to 100kHz	T_J = full range		80		μV
		New chip				290		
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	Legacy chip	f = 120Hz, V_{IN} = 15V to 25V	T_J = full range	40	54		dB
		New chip			40	50		
I_{PK}	Peak output current	Legacy chip	T_J = 25°C			140		mA
		New chip	T_J = 25°C			210		
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	Legacy chip	I_O = 5mA	T_J = 25°C		–1		mV/°C
		New chip	I_O = 5mA	T_J = 25°C		-0.046		
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	Legacy chip	ΔV_O = 2% of V_O	T_J = 25°C		13.7	14.5	V
		New chip	ΔV_O = 2% of V_O	T_J = 25°C		13.7	14	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. Refer to the *Recommended Operating Conditions* table for the operating temperature ranges of legacy and new chip.
(2) Power dissipation ≤ 0.75W.
(3) Recommended minimum load capacitance of 0.01μF to limit high-frequency noise.

5.10 Electrical Characteristics: LM78L15 (Legacy and New Chip)

at specified junction temperature, V_{IN} = 23V, C_{IN} = 0.33μF, C_{OUT} = 0.1μF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
V_O	Output voltage	Legacy chip	T_J = 25°C		14.4	15	15.6	V
			V_{IN} = 17.5V to 30V, and I_O = 1mA to 40mA[2]	T_J = full range	14.25		15.75	
			I_O = 1mA to 70mA[2]		14.25		15.75	
		New chip	T_J = 25°C		14.750	15	15.425	
			V_{IN} = 17.5V to 30V, and I_O = 1mA to 40mA	T_J = full range	14.575		15.450	
			I_O = 1mA to 70mA		14.35		15.45	
V_O	Output voltage	New chip	V_{IN} = 17.5V to 30V, and I_O = 1mA to 40mA	T_J = -40°C to 140°C	14.575		15.450	V
			I_O = 1mA to 70mA		14.35		15.45	

at specified junction temperature, V_{IN} = 23V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
ΔV_O	Line regulation	Legacy chip	V_{IN} = 17.5V to 30V	T_J = 25°C		37	250	mV
			V_I = 20V to 30V			25	140	
		New chip	V_{IN} = 17.5V to 30V			65	92	
			V_I = 20V to 30V			58	65	
	Load regulation	Legacy chip	I_O = 1mA to 100mA	T_J = 25°C		35	150	mV
			I_O = 1mA to 40mA			12	75	
		New chip	I_O = 1mA to 100mA			37	70	
			I_O = 1mA to 40mA			15	60	
I_Q	Quiescent current	Legacy chip	T_J = 25°C			3	5	mA
		New chip	T_J = 25°C			4.1	5.3	
			T_J = 125°C				5.5	
ΔI_Q	Quiescent current change	Legacy chip	V_{IN} = 20V to 30V	T_J = full range			1	mA
			I_O = 1mA to 40mA				0.1	
		New chip	V_{IN} = 20V to 30V				0.47	
			I_O = 1mA to 40mA				0.01	
V_n	Output noise voltage	Legacy chip	f = 10Hz to 100kHz	T_J = 25°C		90		µV
		New chip				388		
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	Legacy chip	f = 120Hz, V_{IN} = 18.5V to 28.5V	T_J = 25°C	37	51		dB
		New chip			40	45		
I_{PK}	Peak output current	Legacy chip	T_J = 25°C			140		mA
		New chip	T_J = 25°C			210		
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	Legacy chip	I_O = 5mA	T_J = 25°C		–1.3		mV/°C
		New chip	I_O = 5mA	T_J = 25°C		-0.079		
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	Legacy chip	ΔV_O = 2% of V_O	T_J = 25°C		16.7	17.5	V
		New chip	ΔV_O = 2% of V_O	T_J = 25°C		16.7	17	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. Refer to the *Recommended Operating Conditions* table for the operating temperature ranges of legacy and new chip.
(2) Power dissipation ≤ 0.75W.

5.11 Electrical Characteristics: LM78L62 (Legacy Chip Only)

at specified junction temperature, V_{IN} = 12V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)(1) (2)

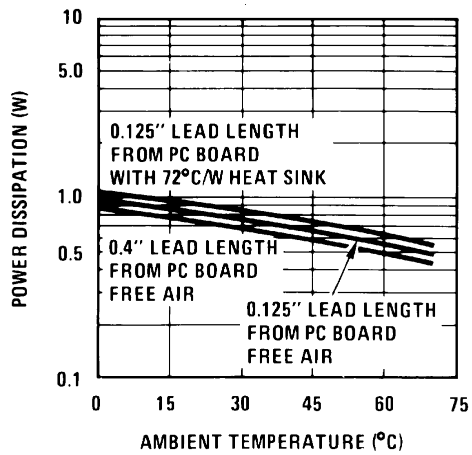
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C		5.95	6.2	6.45	V
		V_{IN} = 8.5V to 20V, and I_O = 1mA to 40mA(3)	T_J = full range	5.9		6.5	
		I_O = 1mA to 70mA(3)		5.9		6.5	
ΔV_O	Line regulation	V_{IN} = 8.5V to 20V	T_J = 25°C		65	175	mV
		V_{IN} = 9V to 20V			55	125	
	Load regulation	I_O = 1mA to 100mA	T_J = 25°C		13	80	mV
		I_O = 1mA to 40mA			6	40	
I_Q	Quiescent current	T_J = 25°C			2	5.5	mA
ΔI_Q	Quiescent current change	V_{IN} = 8V to 20V	T_J = full range			1.5	mA
		I_O = 1mA to 40mA				0.1	
V_n	Output noise voltage(4)	f = 10Hz to 100kHz	T_J = 25°C		50		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120Hz, V_{IN} = 10V to 20V	T_J = 25°C	40	46		dB
		T_J = 25°C			140		
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5mA	T_J = 25°C		-0.75		mV/°C

at specified junction temperature, V_{IN} = 12V, C_{IN} = 0.33µF, C_{OUT} = 0.1µF and I_O = 40mA (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	ΔV_O = 2% of V_O	T_J = 25°C		7.9		V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are verified by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75W.
(4) Recommended minimum load capacitance of 0.01µF to limit high-frequency noise.

5.12 Typical Characteristics



LP Package

Figure 5-1. Maximum Average Power Dissipation

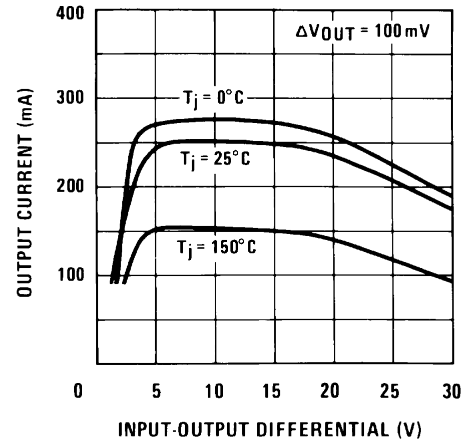


Figure 5-2. Peak Output Current

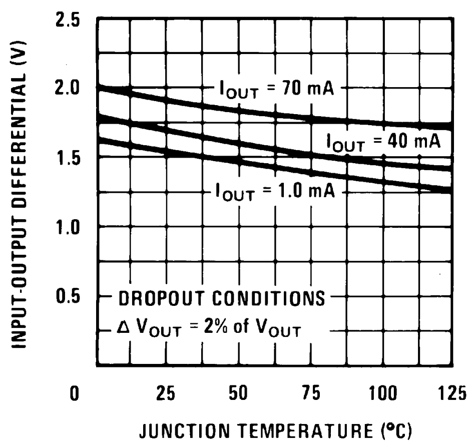


Figure 5-3. Dropout Voltage

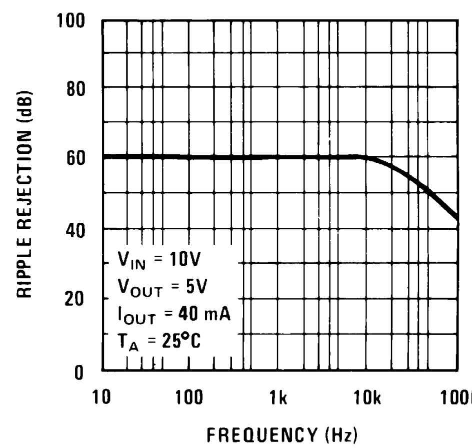


Figure 5-4. Ripple Rejection

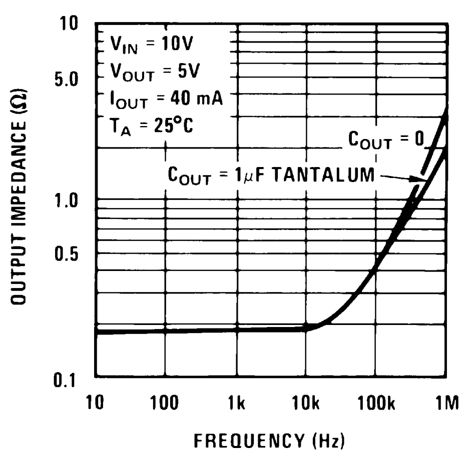


Figure 5-5. Output Impedance

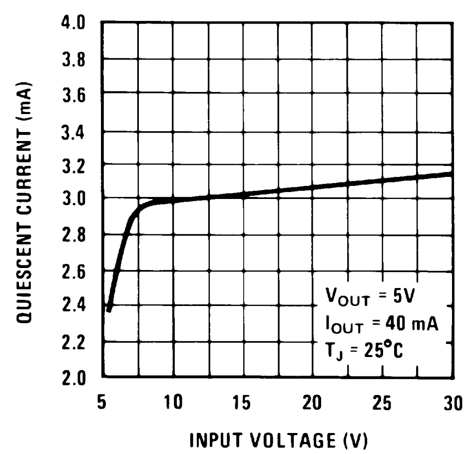


Figure 5-6. Quiescent Current

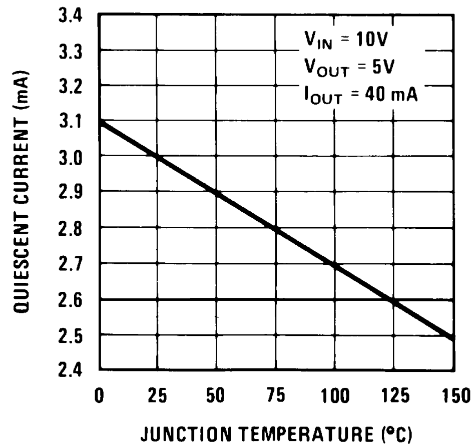


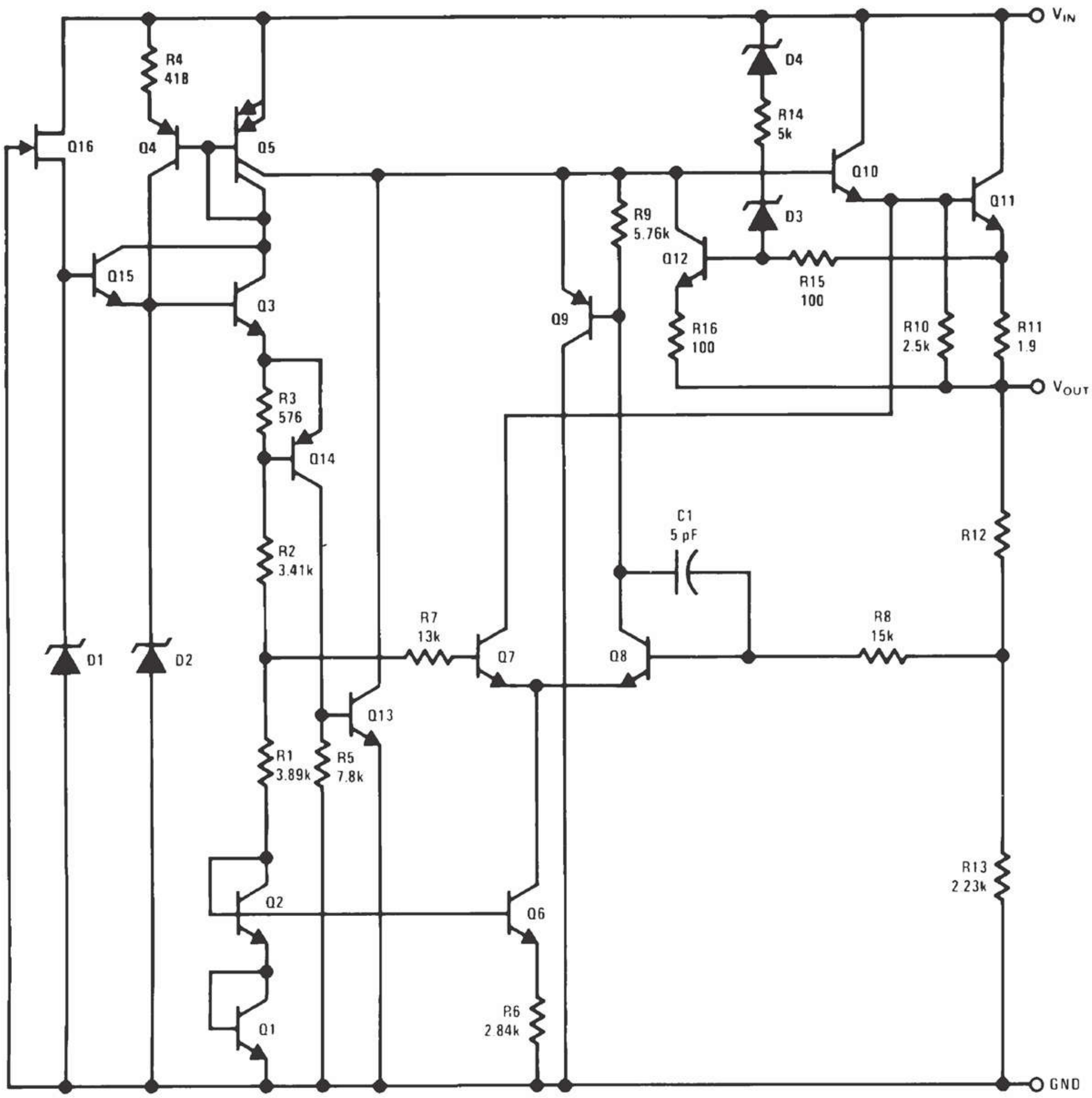
Figure 5-7. Quiescent Current

6 Detailed Description

6.1 Overview

The LM78Lxx series of positive regulators is available in fixed output voltages 5V, 6.2V, 8.2V, 9V, 12V, 15V for the legacy chip, and 3.3V, 5V, 6V, 12V, 15V for the new chip. The regulator can be configured to an adjustable output by connecting the GND pin to the center of a resistive voltage divider as shown in Figure 7-5. In this configuration, the fixed output voltage acts as the reference voltage across R1 allowing the output to be adjusted by changing the resistor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Load Regulation

These devices regulate the voltage between the VOUT and GND pins. Refer to the relevant *Electrical Characteristics* table for details on the load regulation of each output voltage variant.

6.3.2 Protection

The LM78Lxx series of regulators has internal thermal overload protection that automatically shuts off the device if the operating temperature becomes too high. The device also has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events.

6.4 Device Functional Modes

Device Functional Mode Comparison provides a comparison between the normal and dropout modes of operation. Note that if the device junction temperature becomes too high, thermal shutdown disables the device until the device has sufficiently cooled, regardless of V_{IN} and I_O conditions.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_O
Normal	$V_{IN} > V_{IN(MIN)}$	$I_O < I_{PK}$
Dropout	$V_{IN} < V_{IN(MIN)}$	$I_O < I_{PK}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the minimum input voltage required to maintain line regulation ($V_{IN(MIN)}$)
- The output current is less than the current limit ($I_O < I_{PK}$)
- The device junction temperature is within the range specified in the *Recommended Operating Conditions*

6.4.2 Dropout Operation

If the input voltage is lower than the specified minimum value of input voltage required to maintain line regulation ($V_{IN(MIN)}$), but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{IN(MIN)}$, directly after being in a normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than $V_{IN(MIN)}$, the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.3 Shutdown

The device automatically shuts down if the output current or the internal temperature of the device becomes too high.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

These devices are versatile and high-performance regulators with a wide temperature range and tight line and load regulation. An input capacitor is required if the regulator is placed more than 3 inches from the power supply filter. TI recommends a minimum load capacitor of 0.1µF to limit high frequency.

7.2 Typical Applications

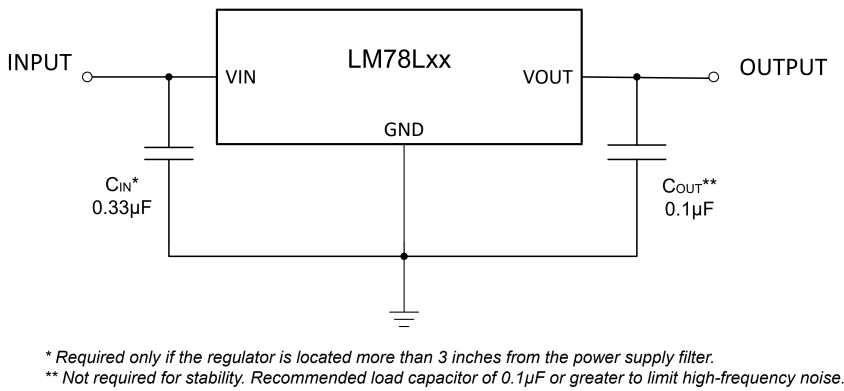


Figure 7-1. Fixed Output Regulator Circuit

7.2.1 Design Requirements

The GND pin must be tied to ground to set VOUT to the desired fixed output voltage. Although not required for stability, a 0.33µF bypass capacitor is recommended on the input, and a 0.1µF bypass capacitor is recommend on the output.

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitor

An input capacitor is only required if the regulator is placed more than 3 inches from the power supply filter. However, an input capacitor is generally recommended to counteract the effect of source resistance and inductance. A 0.33µF capacitor on the input is suitable for most applications.

7.2.2.2 Output Capacitor

An output capacitor is not required for stability. However, TI recommends a minimum load capacitor value of 0.1µF to improve the load and line transient performance of the LM78Lxx regulator.

7.2.2.3 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_I - V_O) \times I_O \quad (1)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{θJA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (2)$$

Thermal resistance ($R_{θJA}$) highly depends on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance application note*, $R_{θJA}$ can be improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

7.2.2.4 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter ($ψ_{JT}$) and junction-to-board characterization parameter ($ψ_{JB}$). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter ($ψ_{JT}$) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter ($ψ_{JB}$) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \quad (3)$$

$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2.2.5 Overload Recovery

As the input voltage rises when power is first turned on, the output follows the input, allowing the regulator to start up into very heavy loads. The input-to-output voltage differential is small during start up when the input voltage is rising, allowing the regulator to supply large output currents.

However, if input voltage is high, a problem can occur such that the output voltage does not recover when removing an output short. Other regulators also exhibit this phenomenon, so the behavior is not unique to the LM78Lxx.

The problem happens with a heavy output load, when the input voltage is high and the output voltage is low. The most common situation in which this can occur is immediately after removing a short circuit. The load line for such a load has the possibility to intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. Because of this double intersection, the input power supply can possibly need to be cycled down to zero and then brought up again to make the output recover to the desired voltage operating point.

7.2.2.6 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the emitter-base junction of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 7-2 shows one approach for protecting the device.

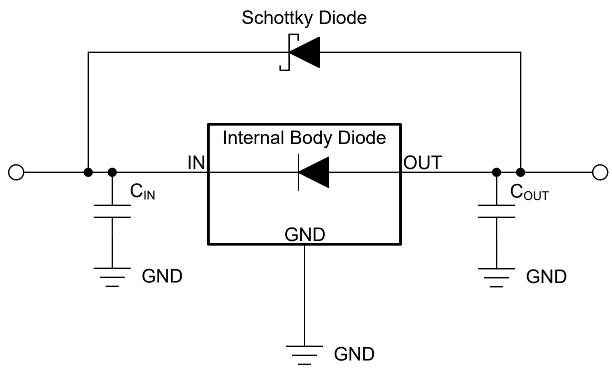


Figure 7-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.7 Polarity Reversal Protection

In many applications, a voltage regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of the opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). During start-up and short-circuit events, this connection can lead to polarity reversal of the regulator output and can damage the internal components of the regulator.

To avoid polarity reversal on the regulator output, use external protection to protect the device.

Figure 7-3 shows one approach for protecting the device.

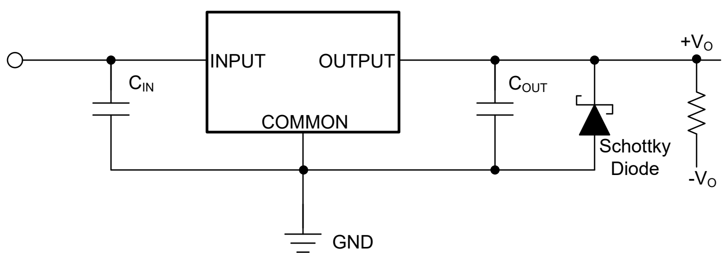


Figure 7-3. Example Circuit for Polarity Reversal Protection Using a Schottky Diode

7.2.3 Application Curve

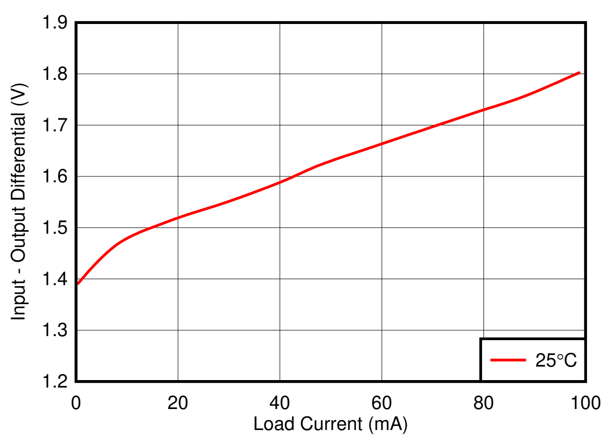
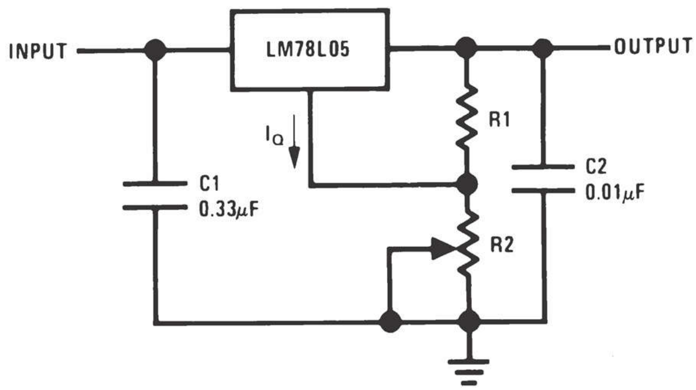


Figure 7-4. LM78Lxx Dropout

7.2.4 Other Application Circuits

Figure 7-5 to Figure 7-9 show application circuit examples using the LM78Lxx devices. Customers must fully validate and test these circuits before implementing a design based on these examples.



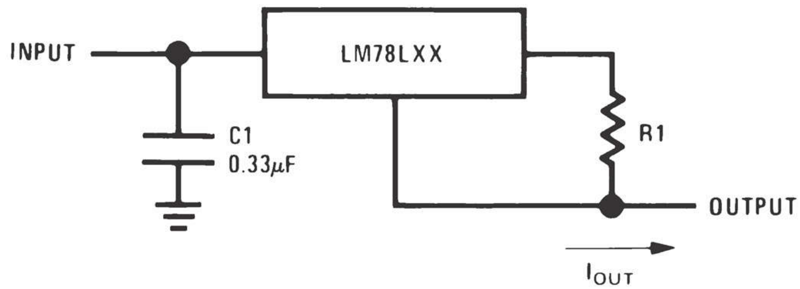
$V_O = 5V + (5V / R1 + I_Q) \times R2^*$

* The 5V represents the fixed output voltage of the LM78L05. If using one of the other LM78Lxx devices, use that fixed output voltage value when calculating V_O.

$I_Q < 5V / (3 \times R1)$

Load regulation (L_R) of LM78L05 ≅ (R1 + R2) / R1

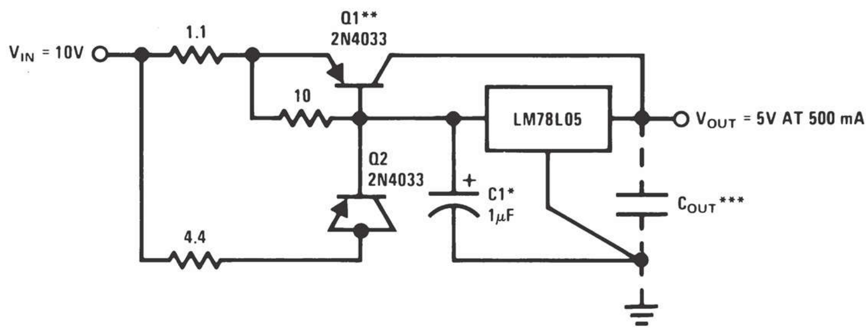
Figure 7-5. Adjustable Output Regulator Circuit



$I_{OUT} = (V_O / R1) + I_Q$

I_Q = 1.5mA over line and load changes

Figure 7-6. Current Regulator Circuit



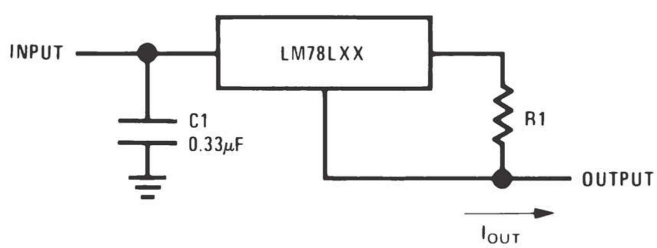
*Solid tantalum

**Heat sink Q1

***Optional: Improves ripple rejection and transient response.

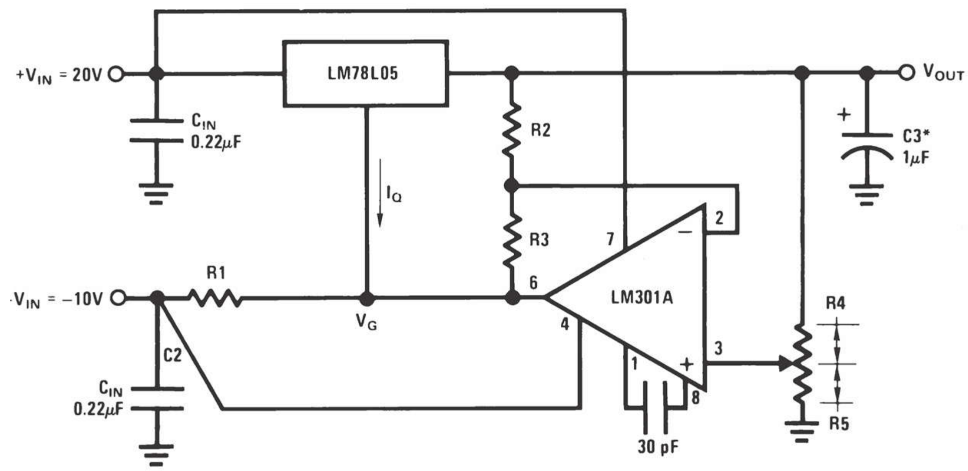
Load Regulation = 0.6%, I_L = 0mA to 250mA pulsed with t_{ON} = 50ms.

Figure 7-7. 5V, 500mA Regulator With Short-Circuit Protection Circuit



*Solid tantalum

Figure 7-8. ±15V, 100mA Dual Power Supply Circuit



*Solid tantalum

$V_O = V_G + 5V$, $R1 = (-V_{IN} / I_{Q(LM78L05)})$

$V_O = 5V (R2 / R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output corresponds to (R2 / R4) = 0.1, (R3 / R4) = 0.9

Figure 7-9. Variable Output Regulator Circuit (0.5V to 18V)

7.3 Power Supply Recommendations

The linear regulator input supply must not exceed the maximum input voltage allowed by the device. The minimum input voltage required to maintain line regulation ($V_{IN(MIN)}$) must be met with extra headroom when possible to keep the output well regulated.

While not required, TI recommends a 0.33μF or higher capacitor be placed at the input to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.

7.4 Layout

7.4.1 Layout Guidelines

Place bypass capacitors as close to the LM78Lxx as possible.

Keep traces short and wide to reduce the amount of parasitic elements in the system, especially at the input and output pins. The actual length and thickness of traces depends on the current carrying capability and heat dissipation required by the end system.

Additional copper and vias connected to ground facilitate additional thermal dissipation, improving the effective thermal resistance of the device and preventing the device from reaching thermal overload. With PCB board layout optimization, RθJA can be improved by 35% to 55% compared to the values found in the Thermal Information table. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note for more details.

7.4.2 Layout Example

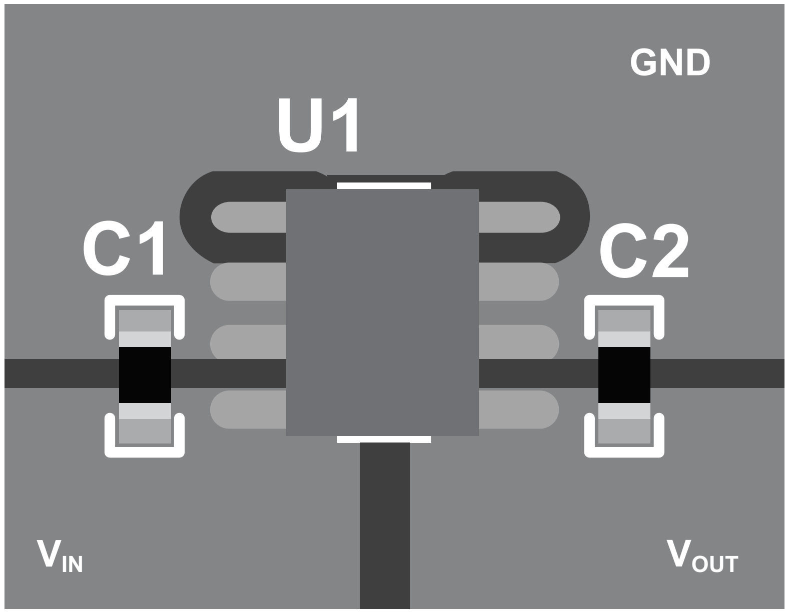


Figure 7-10. LM78Lxx Example Circuit Layout, SOIC Package

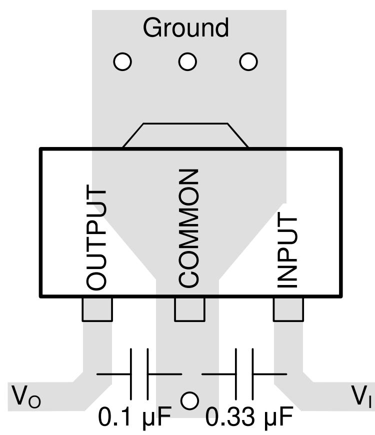


Figure 7-11. LM78Lxx Example Circuit Layout, SOT-89 Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the LM78Lxx. UA78LEVM-075 EVM and related user guide can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.2 Device Nomenclature

PRODUCT	V_{OUT}
LM78L**xx**PKR SOT-89 package, new chip only	**xx** is the nominal output voltage (for example, 33 = 3.3V, 05 = 5.0V, 15 = 15.0V, …). **PK** is the package designator for SOT-89. **R** is the package quantity (R = large reel).
LM78L**xx*yy*** M ***(X)*(/NOPB)** SOIC package, new chip only	**xx** is the nominal output voltage (for example, 33 = 3.3V, 05 = 5.0V, 15 = 15.0V, …). ***yy*** is the junction temperature range designator (AC and AI = -40°C to 125°C). **M** is the package designator (M = SOIC). **(X)** indicates the package quantity (no X = tube, X = large reel). **/NOPB** indicates that the device is lead free.
LM78L**xx*yy*** M ***(X)*(/NOPB)** SOIC package, legacy chip only	**xx** is the nominal output voltage (for example, 05 = 5.0V, 62 = 6.2V, 15 = 15.0V, …). ***yy*** is the junction temperature range designator (AC = 0°C to 125°C, AI = -40°C to 125°C). **M** is the package designator (M = SOIC). **(X)** indicates the package quantity (no X = tube, X = large reel). **/NOPB** indicates that the device is lead free.
LM78L**xx**ACZ/ ***yyyy*** TO-92 package, legacy chip only	**xx** is the nominal output voltage (for example, 05 = 5.0V, 12 = 12.0V, 15 = 15.0V, …). ***AC*** is the junction temperature range designator (AC = 0°C to 125°C). **Z** is the package designator (Z = TO-92). ***yyyy*** indicates the packing method and package quantity (LFT1, LFT7 = large reel, LFT3, LFT4 = ammo pack, NOPB = bulk). All LM78Lxx TO-92 devices are lead free. See the TO-92 Packing Options / Ordering Instructions application note for more packing details.
LM78L**xx**ITP ***(X)*(/NOPB)** DSBGA package, legacy chip only	**xx** is the nominal output voltage (for example, 05 = 5.0V, 09 = 9.0V, …). **ITP** is the package and junction temperature range designator (ITP = DSBGA, -40°C to 85°C). **(X)** indicates the package quantity (no X = small reel, X = large reel). **/NOPB** indicates that the device is lead free.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *UA78L Series Positive-Voltage Linear Regulators* data sheet
- Texas Instruments, *An empirical analysis of the impact of board layout on LDO thermal performance* application note
- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application note
- Texas Instruments, *TO-92 Packing Options/Ordering Instructions* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (June 2020) to Revision M (February 2026) **Page**

- Added new chip (300mm) information, updated formatting....1
- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Updated to include new chip information....1
- Added *Evaluation Module* section....23
- Added nomenclature table....23

Changes from Revision K (December 2016) to Revision L (June 2020) **Page**

- Changed product name to LM78L so document matches product folder....1
- Added first *Features* bullet....1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM78L05ACM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM78L 05ACM
LM78L05ACM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05ACM
LM78L05ACMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM78L 05ACM
LM78L05ACMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05ACM
LM78L05ACZ/LFT1	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT1.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT3.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT4	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT4.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT7	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/LFT7.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05ACZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	Call TI	N/A for Pkg Type	-40 to 125	LM78L 05ACZ
LM78L05AIM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05AM
LM78L05AIM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05AM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM78L05AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05AM
LM78L05AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05AM
LM78L05ITP/NOPB	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	P 03
LM78L05ITP/NOPB.B	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P 03
LM78L05ITPX/NOPB	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	P 03
LM78L05ITPX/NOPB.B	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P 03
LM78L09ITPX/NOPB	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	P 02
LM78L09ITPX/NOPB.B	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P 02
LM78L12ACM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM78L 12ACM
LM78L12ACM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 12ACM
LM78L12ACMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM78L 12ACM
LM78L12ACMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 12ACM
LM78L12ACZ/LFT3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L12ACZ/LFT3.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L12ACZ/LFT4	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L12ACZ/LFT4.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L12ACZ/LFT7	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM78L12ACZ/LFT7.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L12ACZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L12ACZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 12ACZ
LM78L15ACM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM78L 15ACM
LM78L15ACM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 15ACM
LM78L15ACMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM78L 15ACM
LM78L15ACMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM78L 15ACM
LM78L15ACZ/LFT4	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 15ACZ
LM78L15ACZ/LFT4.B	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 15ACZ
LM78L15ACZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 15ACZ
LM78L15ACZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 15ACZ
LM78L62ACZ/NOPB	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 62ACZ
LM78L62ACZ/NOPB.B	Active	Production	TO-92 (LP) | 3	1800 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	LM78L 62ACZ
PLM78L05PKR	Active	Preproduction	SOT-89 (PK) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PLM78L06PKR	Active	Preproduction	SOT-89 (PK) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PLM78L12PKR	Active	Preproduction	SOT-89 (PK) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PLM78L15PKR	Active	Preproduction	SOT-89 (PK) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PLM78L33ACMX/NOPB	Active	Preproduction	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PLM78L33PKR	Active	Preproduction	SOT-89 (PK) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

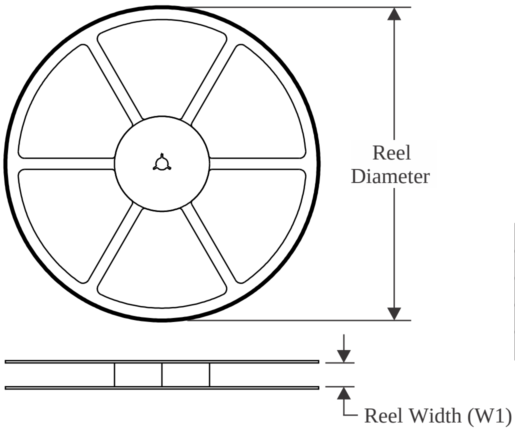
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

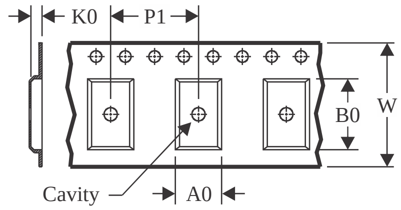
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

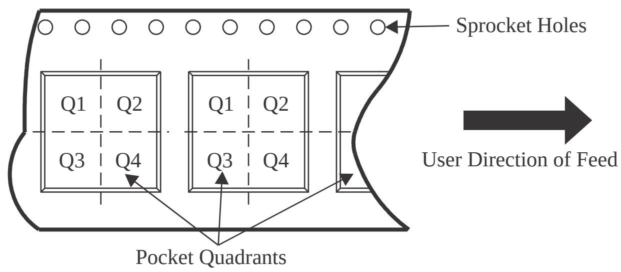


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

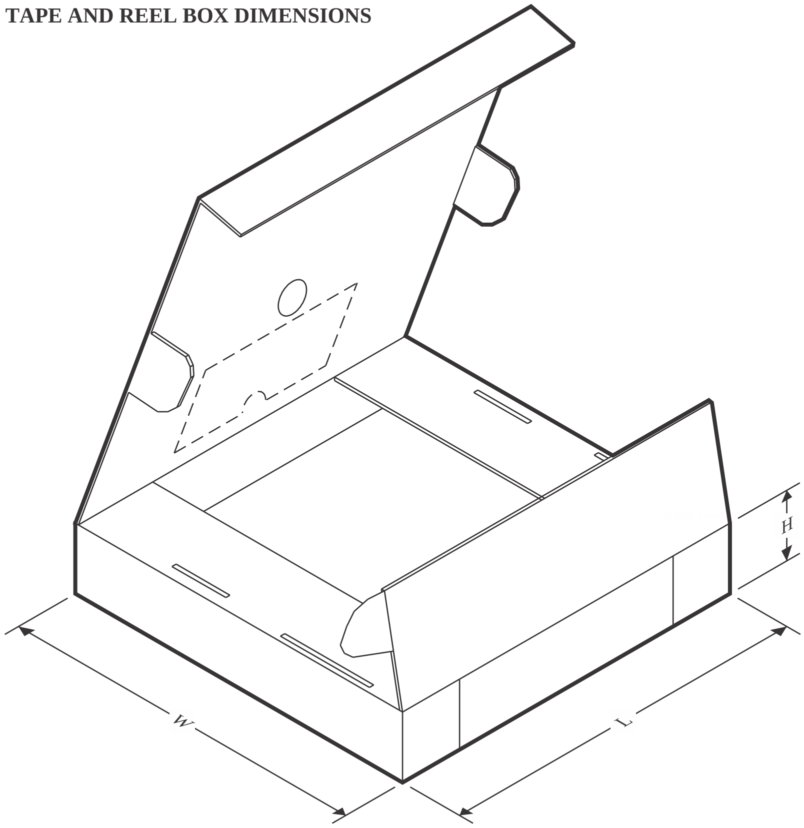
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM78L05ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L05AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L05ITP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM78L05ITPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM78L09ITPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM78L12ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L15ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

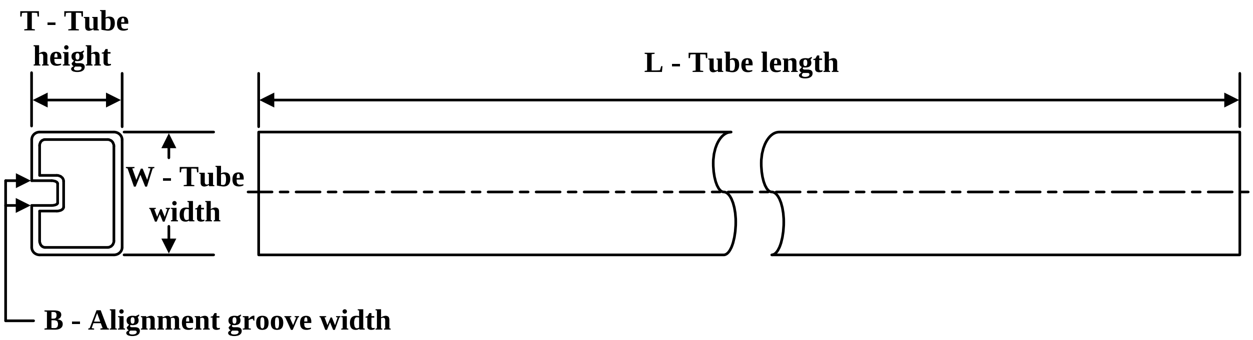
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM78L05ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM78L05AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM78L05ITP/NOPB	DSBGA	YPB	8	250	208.0	191.0	35.0
LM78L05ITPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0
LM78L09ITPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0
LM78L12ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM78L15ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

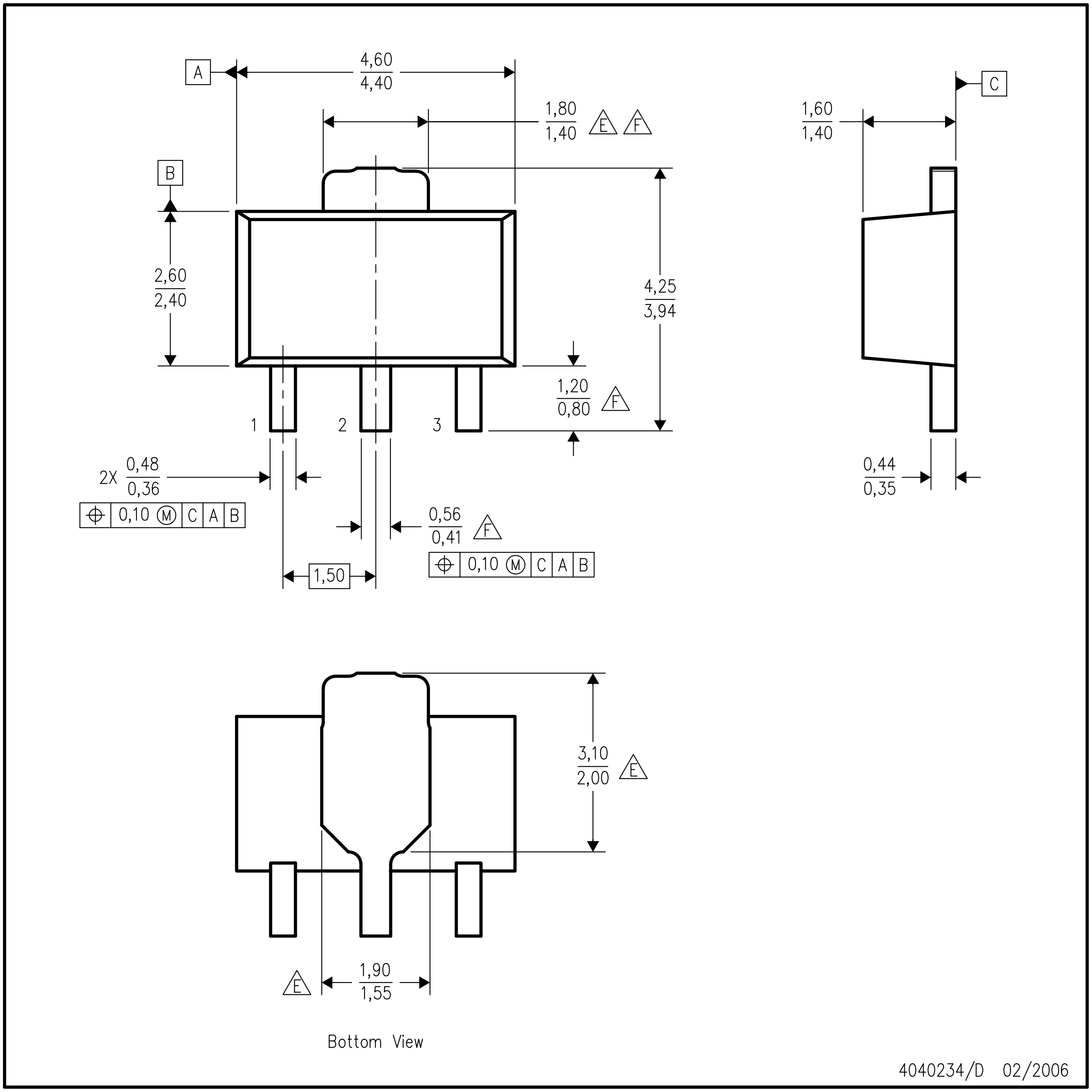
TUBE



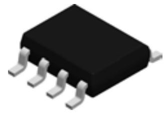
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM78L05ACM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM78L05ACM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM78L05AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM78L05AIM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM78L12ACM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM78L12ACM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM78L15ACM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM78L15ACM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

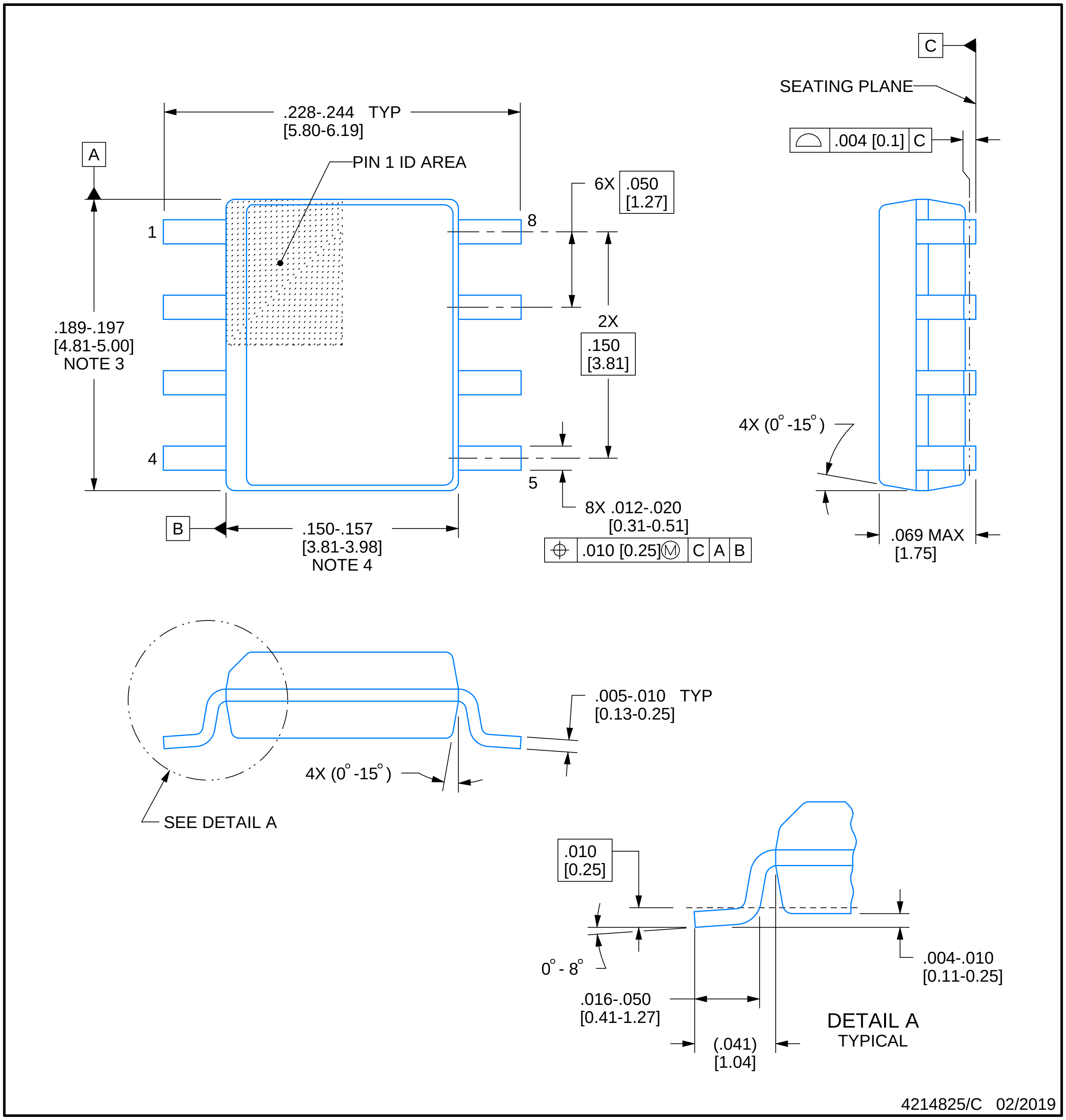


PACKAGE OUTLINE

D0008A

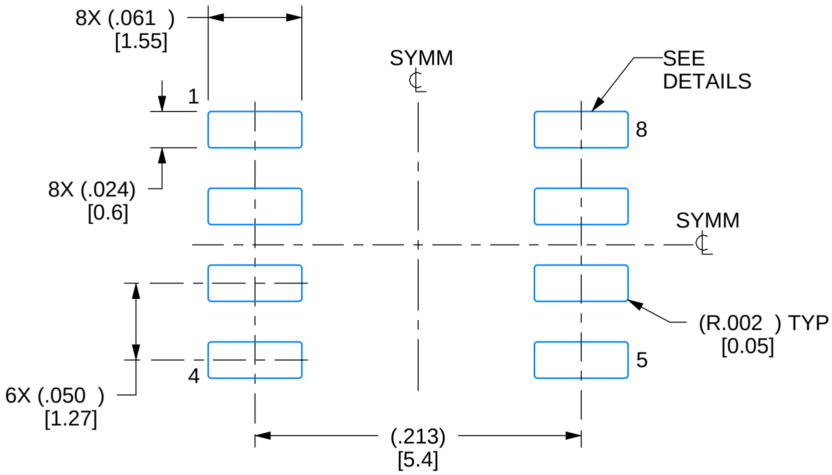
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

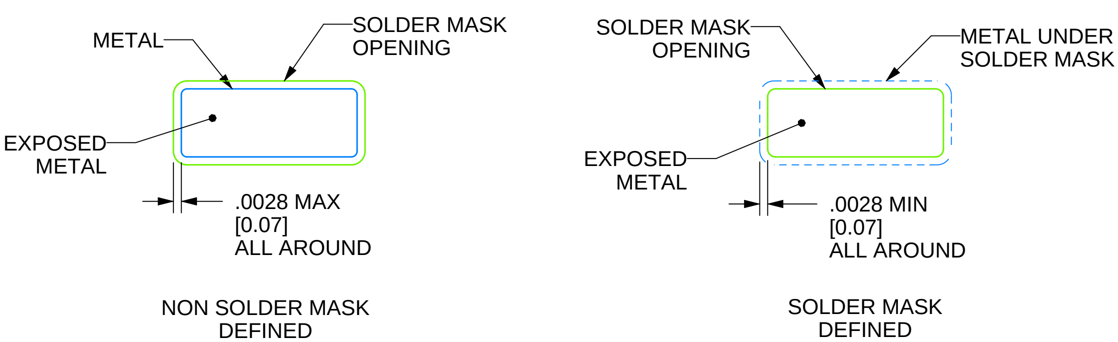


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

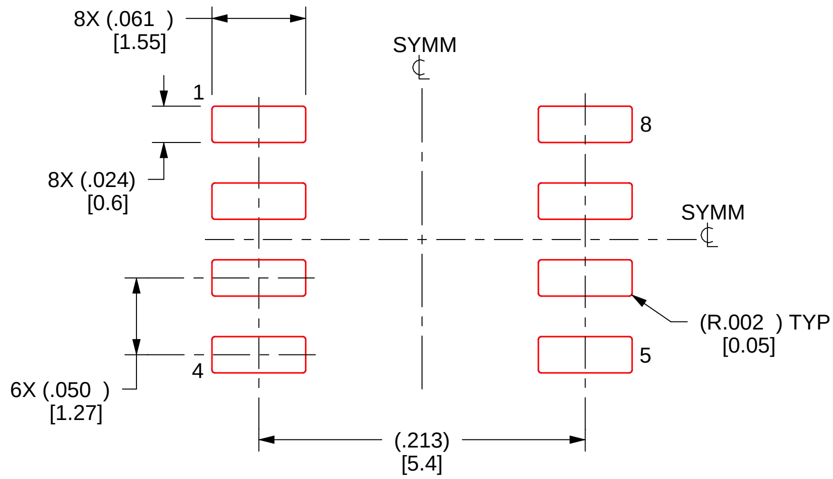


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

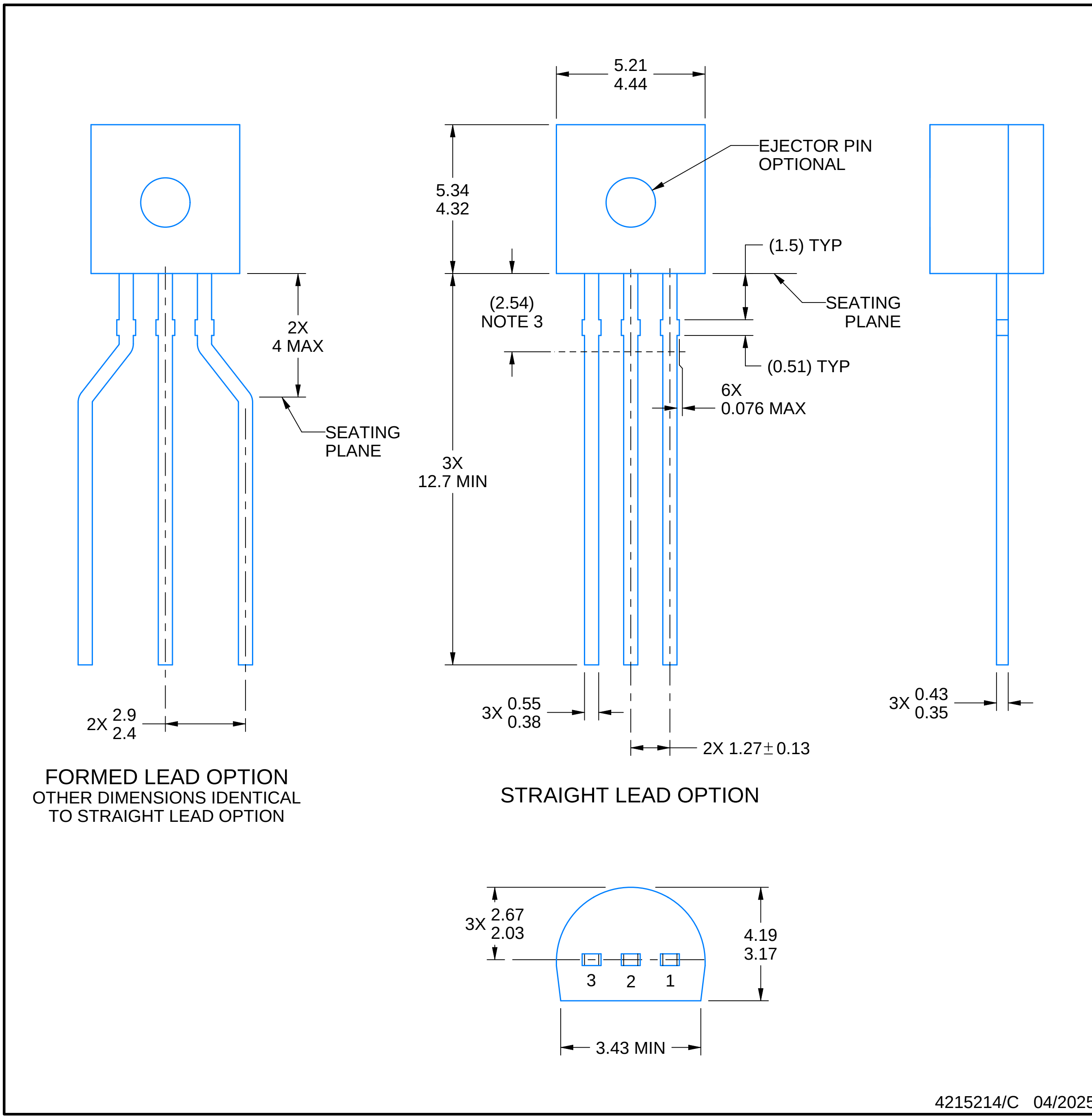
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

LP0003A

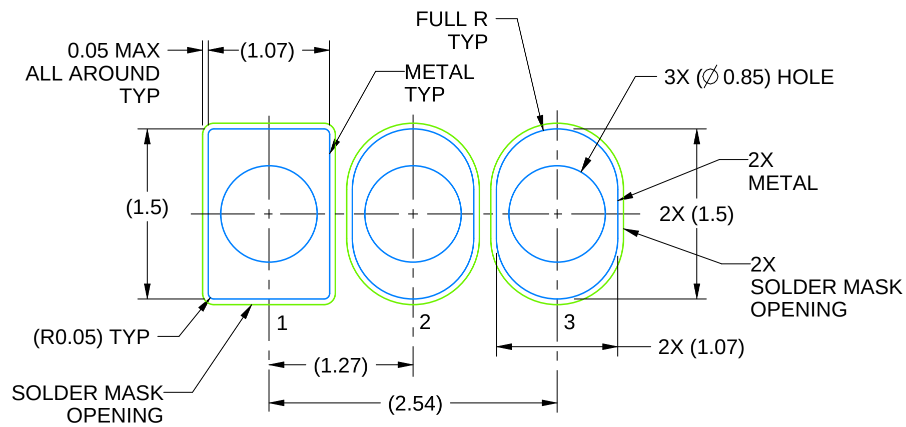
PACKAGE OUTLINE

TO-92 - 5.34 mm max height

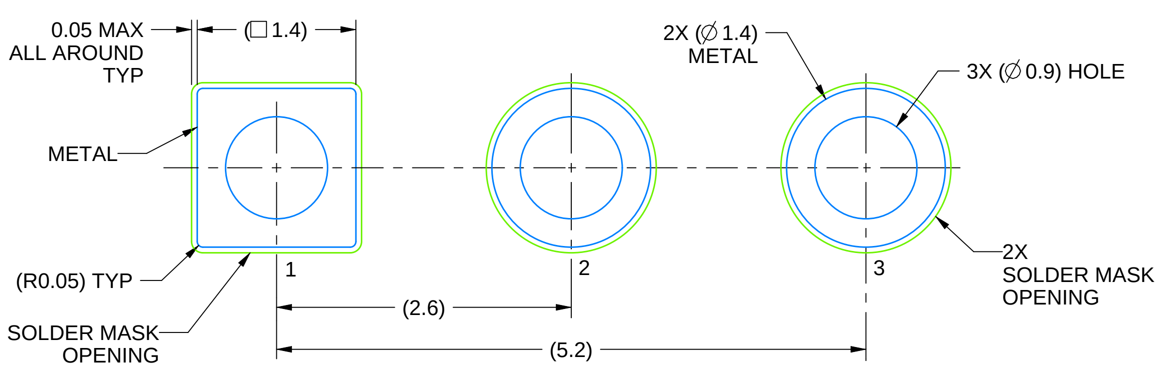


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
    a. Straight lead option available in bulk pack only.
    b. Formed lead option available in tape and reel or ammo pack.
    c. Specific products can be offered in limited combinations of shipping medium and lead options.
    d. Consult product folder for more information on available options.

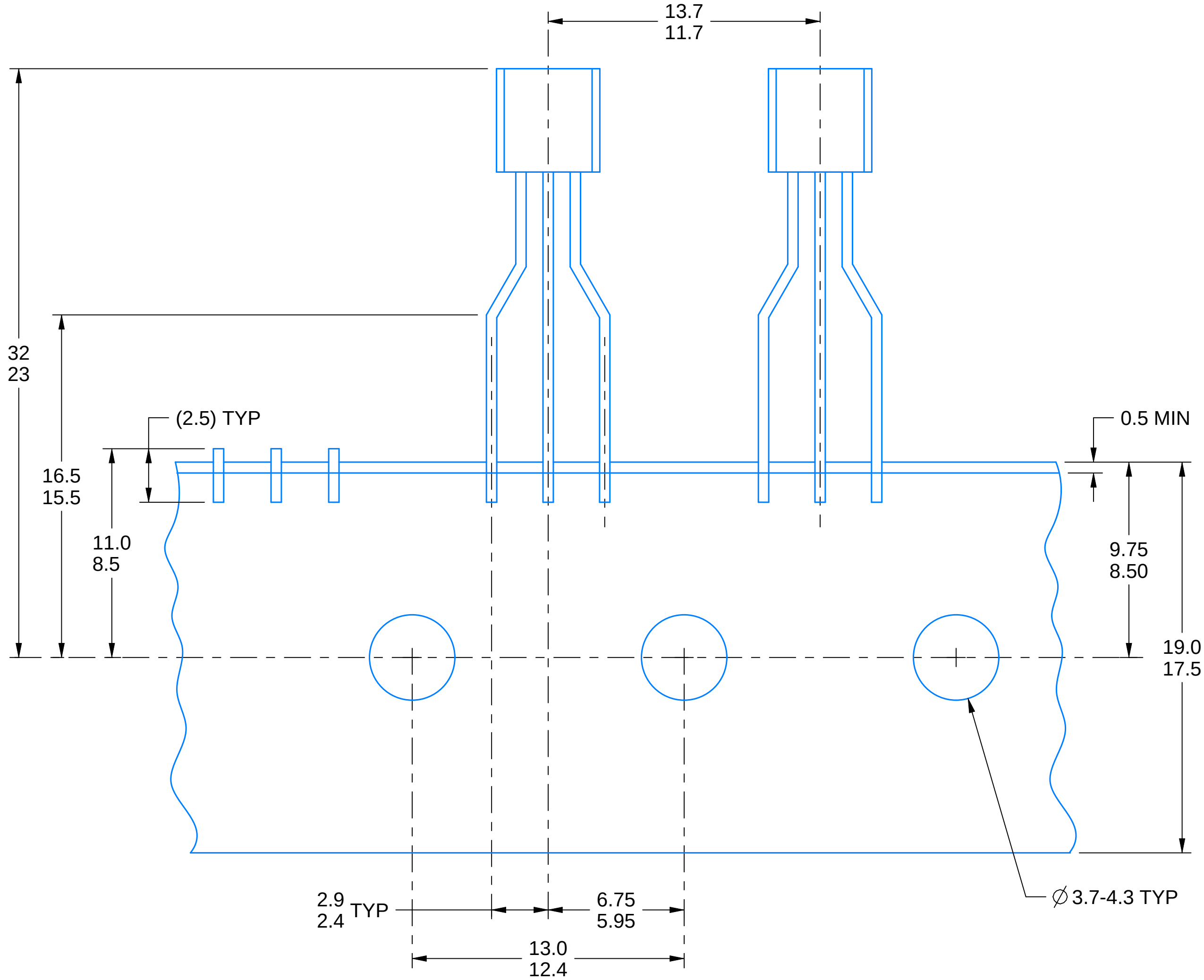


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



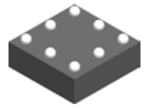
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

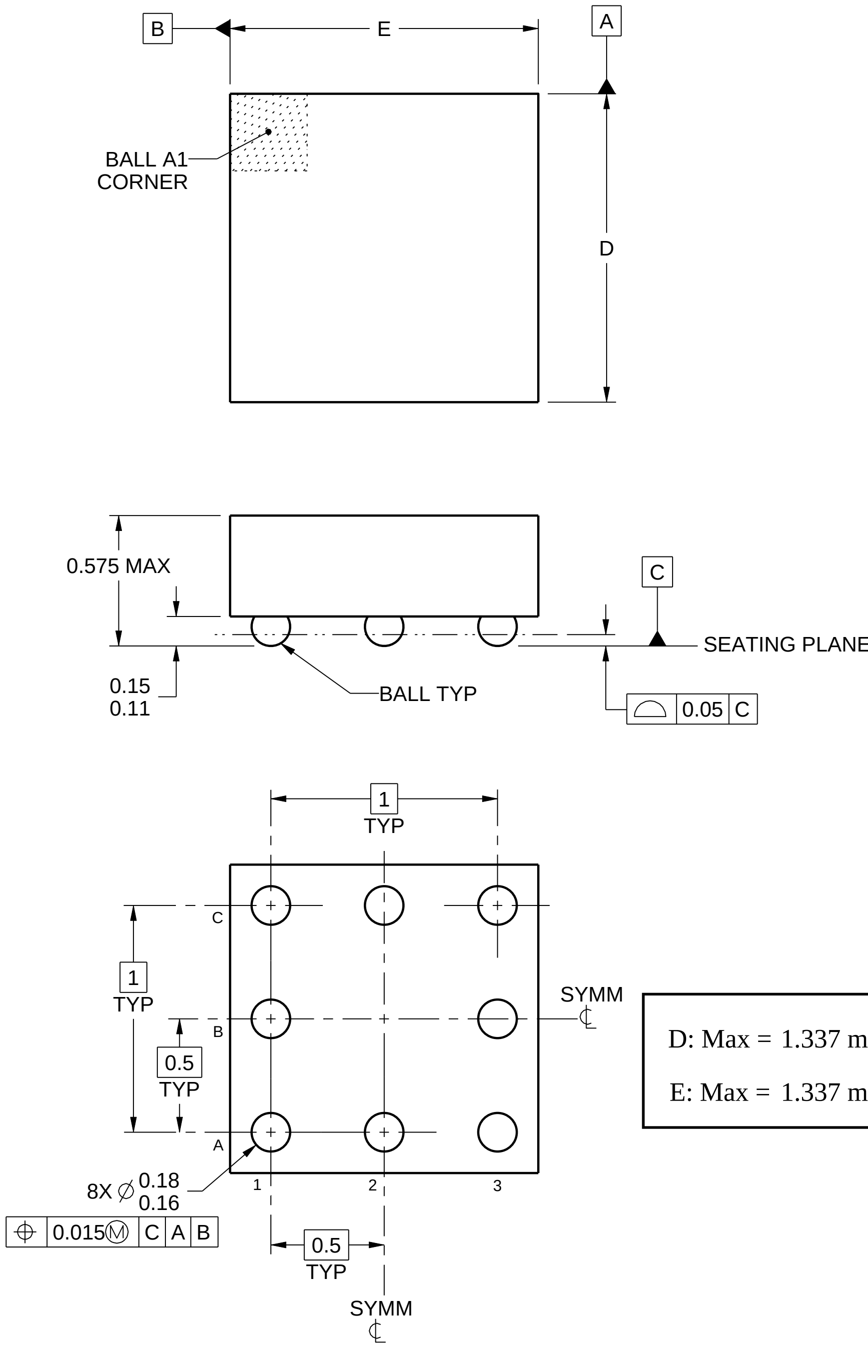
4215214/C 04/2025



FOR FORMED LEAD OPTION PACKAGE

4215214/C 04/2025





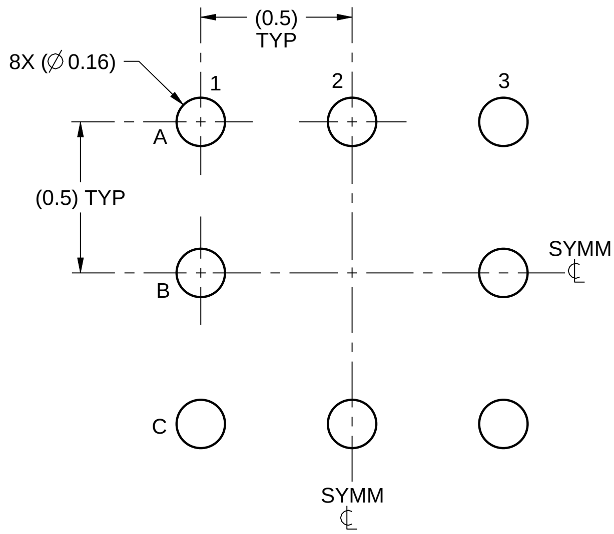
D: Max = 1.337 mm, Min =1.276 mm

E: Max = 1.337 mm, Min =1.276 mm

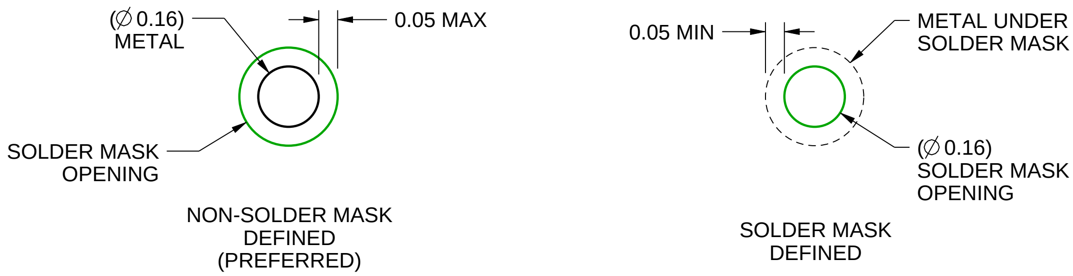
4215100/B 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

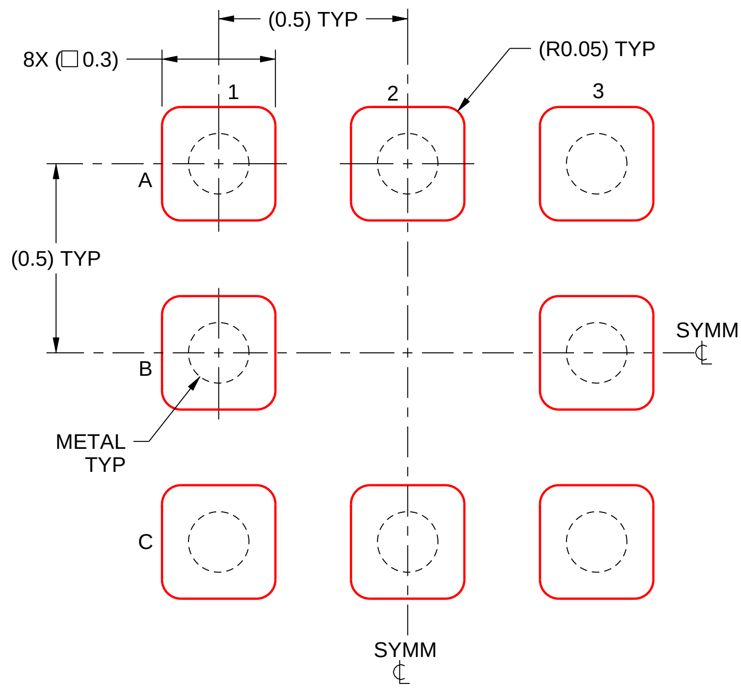


SOLDER MASK DETAILS
NOT TO SCALE

4215100/B 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

4215100/B 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER