SN74HCS125 Quadruple Buffer With 3-State Outputs and Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2V to 6V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100nA
  - Typical input leakage current of ±100 nA
- ±7.8mA output drive at 6V
- Extended ambient temperature range: –40°C to +125°C, T_A

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Debounce a switch
- Eliminate slow or noisy input signals

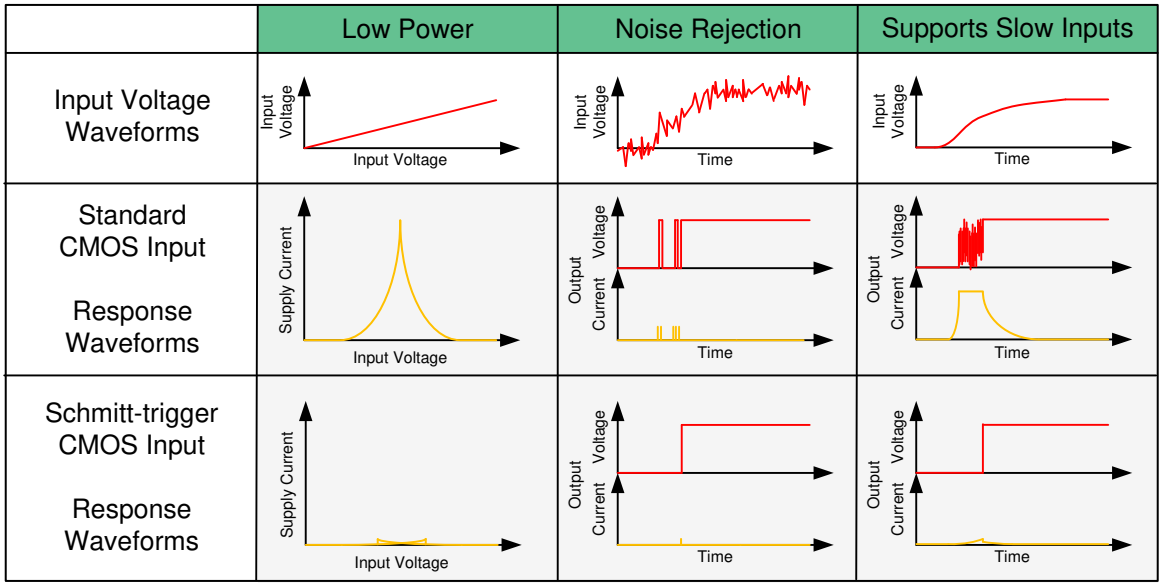
3 Description

The SN74HCS125 contains four independent buffers with 3-state outputs and Schmitt-trigger inputs. Each buffer performs the Boolean function Y = A in positive logic. The outputs can be put into a Hi-Z state by applying a High on the $\overline{OE}$ pin.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74HCS125PW	TSSOP (14)	5.00mm × 4.40mm
SN74HCS125D	SOIC (14)	9.90mm × 3.90mm
SN74HCS125BQA	WQFN (14)	3.00mm × 2.50mm
SN74HCS125DYY	SOT-23-THIN (14)	2.00mm × 4.20mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Benefits of Schmitt-trigger inputs

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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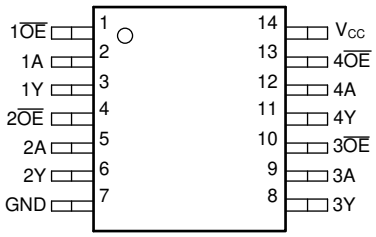
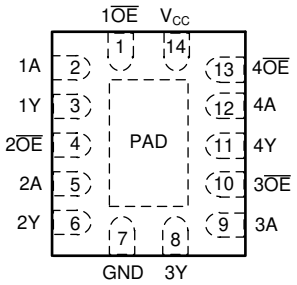
4 Pin Configuration and Functions



D, PW or DYY Package
14-Pin SOIC, TSSOP or SOT
Top View



BQA Package
14-Pin WQFN
Top View

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	2	Input	Channel 1, Input A
1 $\overline{OE}$	1	Input	Channel 1, Output Enable, Active Low
1Y	3	Output	Channel 1, Output Y
2A	5	Input	Channel 2, Input A
2 $\overline{OE}$	4	Input	Channel 2, Output Enable, Active Low
2Y	6	Output	Channel 2, Output Y
3A	9	Input	Channel 3, Input A
3 $\overline{OE}$	10	Input	Channel 3, Output Enable, Active Low
3Y	8	Output	Channel 3, Output Y
4A	12	Input	Channel 4, Input A
4 $\overline{OE}$	13	Input	Channel 4, Output Enable, Active Low
4Y	11	Output	Channel 4, Output Y
GND	7	—	Ground
V_{CC}	14	—	Positive Supply
Thermal Pad[(1)]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) BQA package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current[2]	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
I_{CC}	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	–55		125	°C

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5.4 Thermal Information

THERMAL METRIC[1]		SN74HCS125				UNIT
		PW (TSSOP)	D (SOIC	BQA (WQFN)	DYY (SOT)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	109.7	236.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89	111.0	143.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	77.9	146.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	20.2	29.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	77.8	145.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	56.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2V	1.18		1.3	V
				4.5V	2.39		2.58	
				6V	3.11		3.32	
V_{T-}	Negative switching threshold			2V	0.61		0.66	V
				4.5V	1.31		1.42	
				6V	1.72		1.87	
ΔV_T	V_{T+} - V_{T-}			2V	0.55		0.67	V
				4.5V	1.04		1.21	
				6V	1.34		1.49	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20μA	2V to 6V	V_{CC} - 0.1	V_{CC} - 0.002		V
			I_{OH} = -6mA	4.5V	4.0	4.3		
			I_{OH} = -7.8mA	6V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20μA	2V to 6V		0.002	0.1	V
			I_{OL} = 4mA	4.5V		0.18	0.30	
			I_{OL} = 7.8mA	6V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6V		±100	±1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, I_O = 0		6V		0.1	2	μA
C_i	Input capacitance			2V to 6V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2V to 6V		10		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A	Y	2 V		12	39	ns
				4.5 V		6	26	
				6 V		5	24	

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5.6 Switching Characteristics (continued)

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{en}	Enable time	$\overline{OE}$	Y	2 V		14	24	ns
				4.5 V		7	10	
				6 V		6	9	
t_{dis}	Disable time	$\overline{OE}$	Y	2 V		12	16	ns
				4.5 V		9	10	
				6 V		8	9	
t_t	Transition-time		Any	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

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5.7 Typical Characteristics

T_A = 25°C

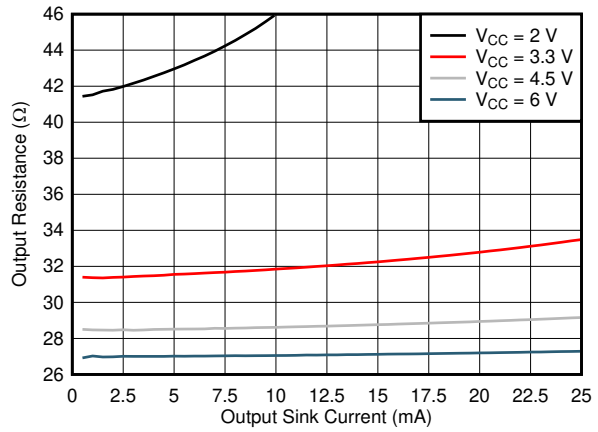


Figure 5-1. Output Driver Resistance in LOW State

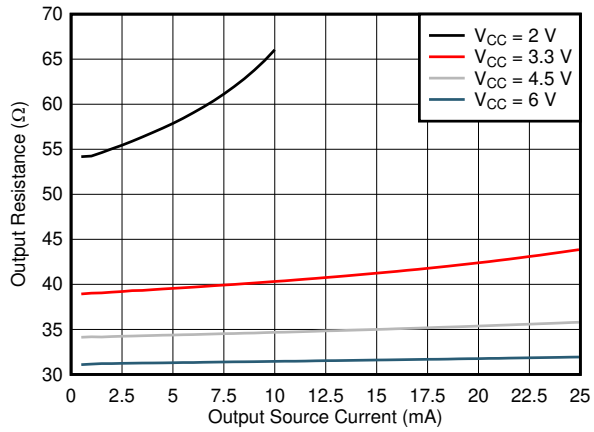


Figure 5-2. Output Driver Resistance in HIGH State

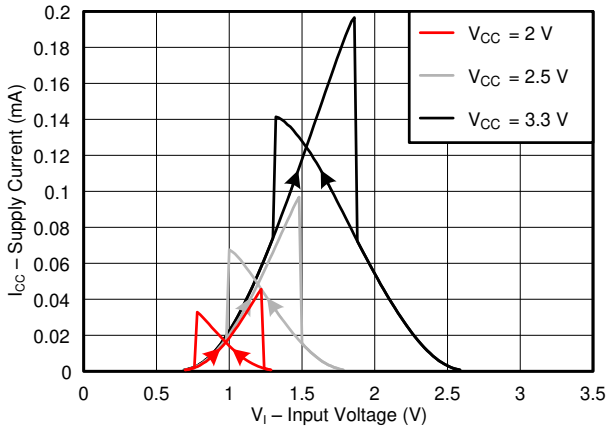


Figure 5-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3V Supply

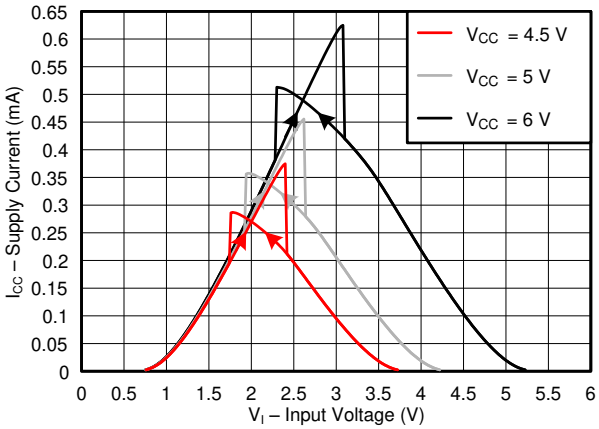


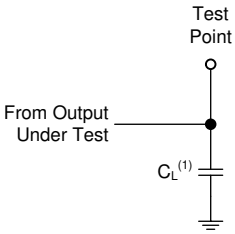
Figure 5-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6V Supply

6 Parameter Measurement Information

Phase relationships between waveforms are selected arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

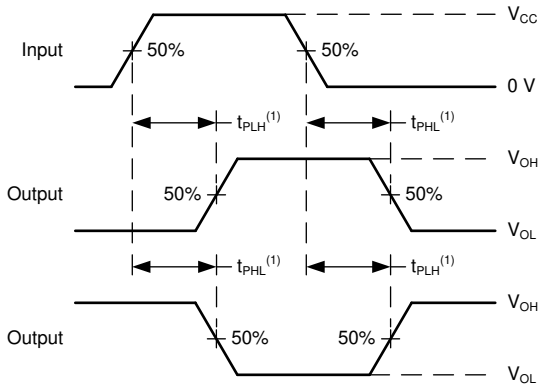
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



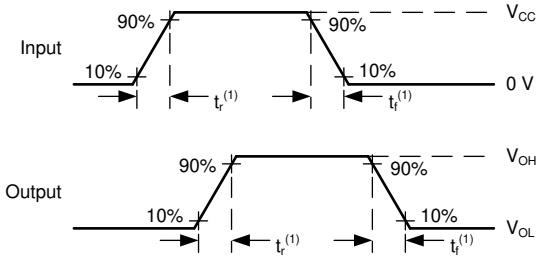
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

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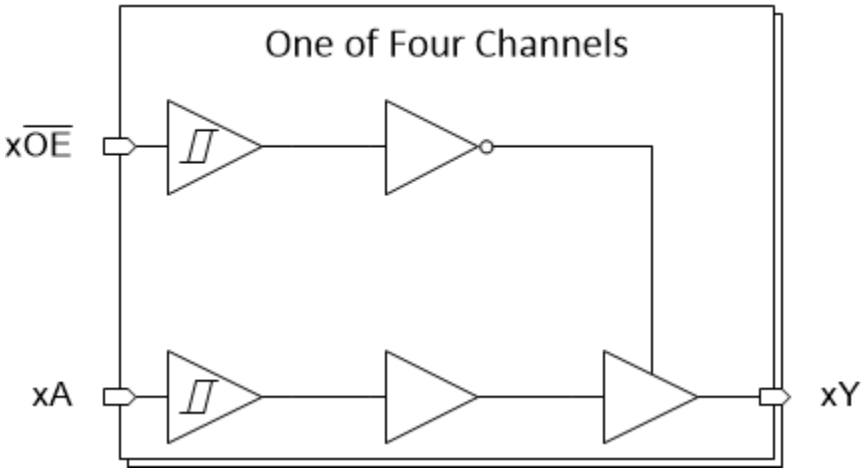
7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs and Schmitt-trigger inputs. Each buffer performs the Boolean function Y = A in positive logic. The outputs can be put into a Hi-Z state by applying a High on the $\overline{OE}$ pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, properly terminating unused inputs is still recommended. Driving the inputs with slow transitioning signals increases dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

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7.3.3 Clamp Diode Structure

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

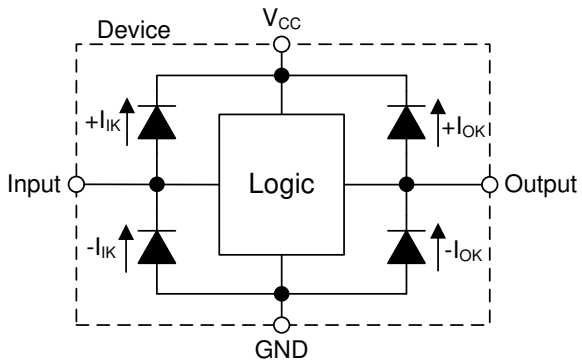

Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Function Table lists the functional modes of the SN74HCS125.

Table 7-1. Function Table

INPUTS(1)		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a buffer with a 3-state output is used to disable a data signal as shown in Figure 8-1. The remaining three buffers can be used for signal conditioning in other places in the system, or the inputs can be grounded and the channels left unused.

8.2 Typical Application

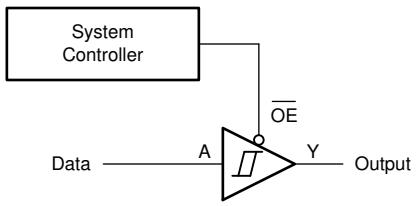

Figure 8-1. Typical application block diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS125 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS125 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74HCS125 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, do not exceed 50pF.

The SN74HCS125 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74HCS125 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74HCS125 has no input signal transition rate requirements because the device has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the Electrical Characteristics . This hysteresis value provides the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the Typical Characteristics .

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Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74HCS125 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

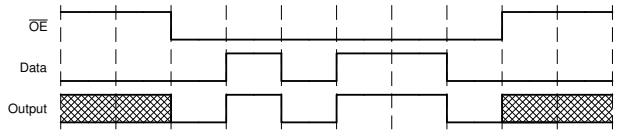

Figure 8-2. Application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. Multiple bypass capacitors can be placed in parallel to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

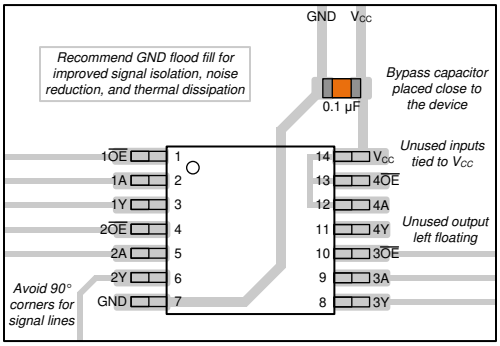

Figure 8-3. Example layout for the SN74HCS125

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *HCMOS Design Considerations* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 1, 2022 to March 19, 2026 (from Revision C (May 2022) to Revision D (March 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed V_{T+} limits at 2V V_{CC} from 0.7V (min), 1.5V (max) to 1.18V (min), 1.3V (max) 5
- Changed V_{T+} limits at 4.5V V_{CC} from 1.7V (min), 3.15V (max) to 2.39V (min), 2.58V (max) 5
- Changed V_{T+} limits at 6V V_{CC} from 2.1V (min), 4.2V (max) to 3.11V (min), 3.32V (max) 5
- Changed V_{T-} limits at 2V V_{CC} from 0.3V (min), 1.0V (max) to 0.61V (min), 0.66V (max).....5
- Changed V_{T-} limits at 4.5V V_{CC} from 0.9V (min), 2.2V (max) to 1.31V (min), 1.42V (max) 5
- Changed V_{T-} limits at 6V V_{CC} from 1.2V (min), 3.0V (max) to 1.72V (min), 1.87V (max).....5
- Changed ΔV_T limits at 2V V_{CC} from 0.2V (min), 1.0V (max) to 0.55V (min), 0.67V (max).....5
- Changed ΔV_T limits at 4.5V V_{CC} from 0.4V (min), 1.4V (max) to 1.04V (min), 1.21V (max).....5
- Changed ΔV_T limits at 6V V_{CC} from 0.6V (min), 1.6V (max) to 1.34V (min), 1.49V (max).....5

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Changes from Revision B (December 2021) to Revision C (May 2022)	Page
• Changed incorrect units for input leakage current from µA to nA	5

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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