TICS100MOD Multi-Protocol Industrial Communication Module

1 Features

- **Multi-Protocol Industrial Ethernet Support**
  - EtherCAT
  - PROFINET
  - EtherNet/IP
- **Dual-Port 10/100 Mbps Ethernet**
  - Two 10/100 Mbps Ethernet ports (optimized for EtherCAT)
  - IEEE 802.3 compliant
- **High-Performance Processor**
  - 500 MHz dual-core Arm Cortex-R5F MCU with real-time control, safety and security
  - Hardware acceleration for real-time protocols (PRU-ICSS)
  - Low latency communication
- **Single Supply**
  - 3.3V ±10% single supply operation
  - CORE_EN pin for module enable
- **Host Interfaces**
  - QSPI (PRU-based), max clock 27 MHz
  - SPI
  - host interrupt lines
- **Industrial Design**
  - Extended temperature range: -40°C to +85°C
  - Pre-certified module approach
  - Compact 30 mm × 18 mm footprint

2 Applications

- Factory automation systems
- Industrial control and monitoring
- Process control equipment
- Robotics and motion control
- Building automation
- Industrial IoT gateways
- PLC communications
- Machine-to-machine (M2M) connectivity

3 Description

The TICS100MOD is an industrial communication module that provides a common API for several fieldbus protocols like **EtherCAT**, **EtherNet/IP** and **PROFINET**. The module will be connected to an external host controller (MCU, Linux board or other SPI-capable controller) through an SPI interface and a few GPIO control signals. The industrial protocol stack runs on the module, so the host application only has to handle application-related data processing.

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4 Functional Block Diagram

The diagram below shows the functional block diagram of the TICS100MOD module.

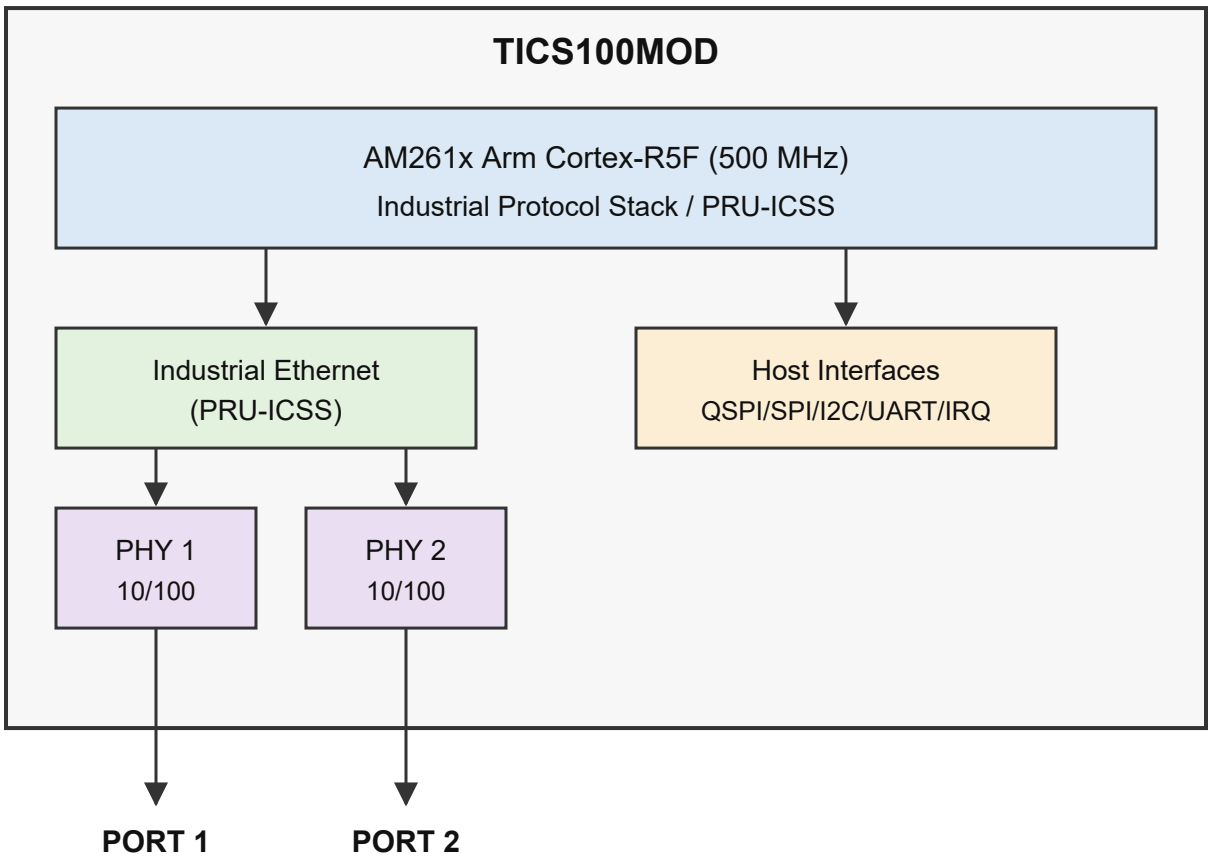


Figure 4-1. TICS100MOD Block Diagram

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5 Pin Configuration and Functions

TICS100MOD Pin Diagram (Top View)

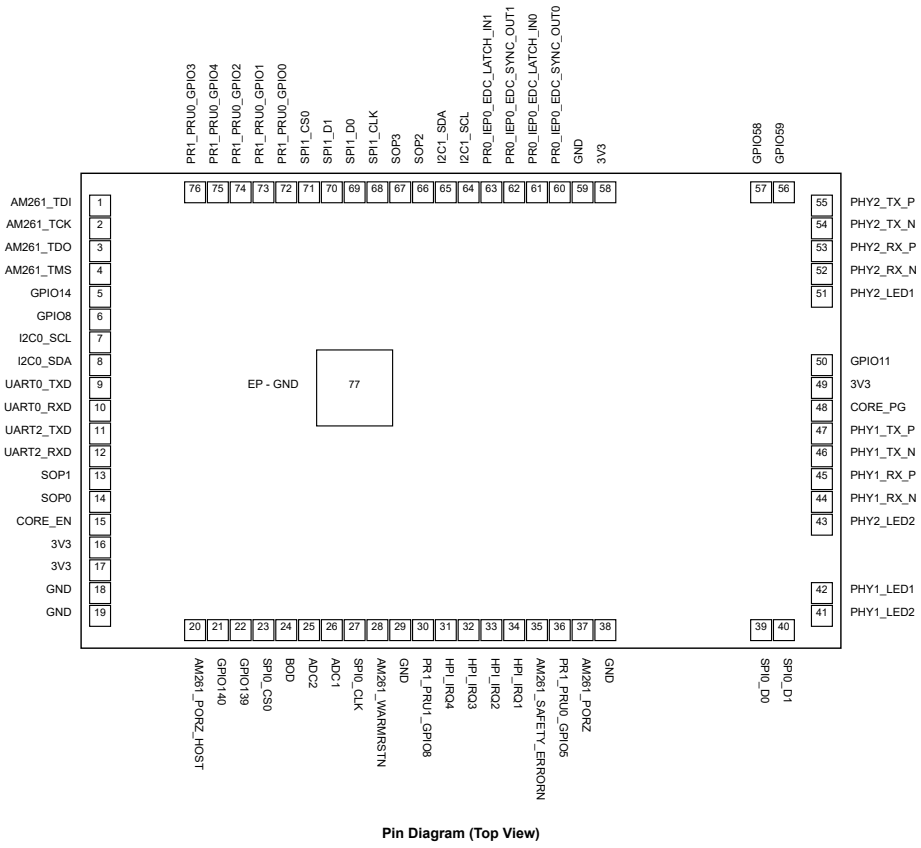


Figure 5-1. Pin Diagram

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
3V3	16, 17, 49, 58	POW	3.3V supply
CORE_EN	15	I	Module core enable
CORE_PG	48	O	Module core power good
GND	18, 19, 29, 38, 59	GND	Ground
EP	77	Power	Exposed pad, ground
PHY1_TX_P	47	Analog	Port 1 differential transmit
PHY1_TX_N	46	Analog	Port 1 differential transmit
PHY1_RX_P	45	Analog	Port 1 differential receive
PHY1_RX_N	44	Analog	Port 1 differential receive
PHY1_LED1	42	O	Port 1 LED 1
PHY1_LED2	41	O	Port 1 LED 2
PHY2_TX_P	55	Analog	Port 2 differential transmit
PHY2_TX_N	54	Analog	Port 2 differential transmit

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Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PHY2_RX_P	53	Analog	Port 2 differential receive
PHY2_RX_N	52	Analog	Port 2 differential receive
PHY2_LED1	51	O	Port 2 LED 1
PHY2_LED2	43	O	Port 2 LED 2
AM261_PORZ	37	I	Power-on reset
AM261_PORZ_HOST	20	I	Power-on reset from host
AM261_WARMRSTN	28	I	Warm reset (active low)
AM261_SAFETY_ERRORN	35	O	Safety error (active low)
SOP3	67	I	Boot mode; must be set before power ramp
SOP2	66	I	Boot mode; must be set before power ramp
SOP1	13	I	Boot mode; must be set before power ramp
SOP0	14	I	Boot mode; must be set before power ramp
AM261_TDI	1	I	JTAG data in
AM261_TCK	2	I	JTAG clock
AM261_TDO	3	O	JTAG data out
AM261_TMS	4	I/O	JTAG mode select
PR1_PRU0_GPIO0	72		QSPI signal
PR1_PRU0_GPIO1	73		QSPI signal
PR1_PRU0_GPIO2	74		QSPI signal
PR1_PRU0_GPIO3	76		QSPI signal
PR1_PRU0_GPIO4	75		QSPI signal
PR1_PRU0_GPIO5	36		QSPI signal
PR1_PRU1_GPIO8	30		QSPI signal
SPI0_CLK	27		SPI0 clock
SPI0_CS0	23		SPI0 chip select 0
SPI0_D0	39		SPI0 data 0
SPI0_D1	40		SPI0 data 1
SPI1_CLK	68		SPI1 clock
SPI1_CS0	71		SPI1 chip select 0
SPI1_D0	69		SPI1 data 0
SPI1_D1	70		SPI1 data 1
I2C0_SCL	7		I2C0 clock
I2C0_SDA	8		I2C0 data
I2C1_SCL	64		I2C1 clock
I2C1_SDA	65		I2C1 data
UART0_TXD	9	O	UART0 transmit
UART0_RXD	10	I	UART0 receive
UART2_TXD	11	O	UART2 transmit
UART2_RXD	12	I	UART2 receive
HPI_IRQ1	34		Host interrupt request 1
HPI_IRQ2	33		Host interrupt request 2
HPI_IRQ3	32		Host interrupt request 3

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Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
HPI_IRQ4	31		Host interrupt request 4
PR0_IEP0_EDC_SYNC_OUT0	60	O	SYNC0 output
PR0_IEP0_EDC_SYNC_OUT1	62	O	SYNC1 output
PR0_IEP0_EDC_LATCH_IN0	61	I	LATCH0 input
PR0_IEP0_EDC_LATCH_IN1	63	I	LATCH1 input
GPIO14	5	I/O	General purpose I/O
GPIO8	6	I/O	General purpose I/O
GPIO11	50	I/O	General purpose I/O
GPIO59	56	I/O	General purpose I/O
GPIO58	57	I/O	General purpose I/O
GPIO140	21	I/O	General purpose I/O
GPIO139	22	I/O	General purpose I/O
ADC1	26	Analog	ADC input
ADC2	25	Analog	ADC input
BOD	24	Analog	Brown-out Detection

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6 Specifications

All specifications are given at the module pins. Typical values are measured with nominal device at 25°C.

Over operating free-air temperature range (unless otherwise noted)

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
3V3	Supply voltage	-0.5	4.2	V
	Input Voltage to all digital pins	-0.5	3V3 + 0.5	V
T_A	Operating ambient temperature	-40	85	°C
T_{stg}	Storage temperature	-40	105	°C

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins	±500	

over operating free-air temperature range (unless otherwise noted)

6.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
3V3	3.3V Supply	2.97	3.3	3.63	V
T_A	Operating ambient temperature	-40		85	°C

6.4 Thermal Resistance Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	°C/W(1)(2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	7.1	N/A
$R\Theta_{JB}$	Junction-to-board	6.7	N/A
$R\Theta_{JA}$	Junction-to-free air	20.7	0
$R\Theta_{JA}$	Junction-to-moving air	14.5	1
		13.3	2
		12.6	3
Ψ_{JT}	Junction-to-package top	0.14	0
		0.40	1
		0.53	2
		0.64	3
Ψ_{JB}	Junction-to-board	6.5	0
		6.0	1
		5.9	2
		5.9	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)

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- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) ℃/W = degrees Celsius per watt
(3) m/s = meters per second

over operating free-air temperature range (unless otherwise noted)

6.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage		0.65 x V_{IO}		V_{IO}	V
V_{IL}	Low Level Input Voltage		0		0.35 x V_{IO}	
V_{OH}	High Level Output Voltage	at 4mA	V_{IO} - 0.45		V_{IO}	
V_{OL}	Low Level Output Voltage	at 4mA	0		0.45	

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7 Detailed Description

7.1 Overview

The TICS100MOD is a compact industrial communication module built around a TI AM261x MCU. It adds industrial networking capability to embedded systems, PLCs, and industrial automation equipment, as a TI-based alternative with smaller footprint and lower BOM cost than comparable communication modules.

The module features two 10/100 Mbps Ethernet ports with integrated low-latency PHYs, enabling communication in EtherCAT, PROFINET, and EtherNet/IP networks. Hardware acceleration in the MCU ensures the deterministic, real-time performance required by industrial automation applications.

The module is supplied from a single 3.3V rail provided by the host through the mating connector. Firmware and configuration are supplied by the host; the module has no external flash or EEPROM.

7.2 Processor Subsystem

7.2.1 Arm Cortex-R5F Subsystem

The R5FSS is a dual-core implementation of the Arm®Cortex®-R5F processor configured for dual-core (split) or lockstep modes of operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm®CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC. The device has one R5FSS module for a total possible 2x functional cores (dual-core mode) or 1x functional cores (lockstep mode).

Note

The Arm®Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating-point Unit (FPU) extension.

For more information, see *R5FSS* section in *Processors and Accelerators* chapter in the device TRM.

7.3 Identification

Table 7-1. Device Identification

Orderable Part Number (OPN)	Package	Size
TICS100MOD	Module	30mm x 18mm x 4.15mm

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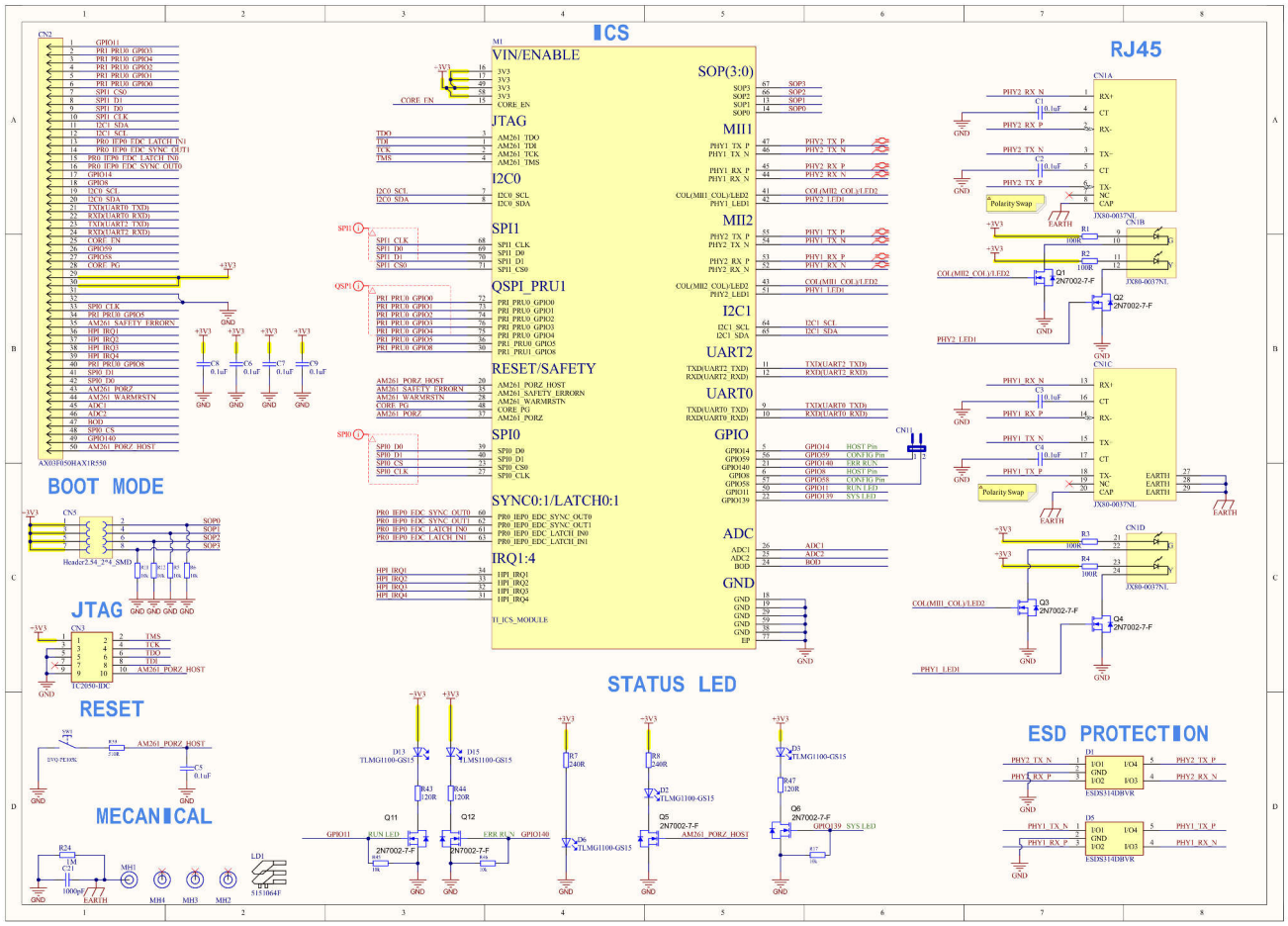
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8 Application Information

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application



8.2 Reset

The module is reset through AM261_PORZ / AM261_PORZ_HOST, for example from a host circuit or button. AM261_WARMRSTN provides a warm reset.

8.3 Boot Modes

The boot mode pins SOP[3:0] provide boot information to the ROM code and must be set up before the power ramp.

Table 8-1. Boot Modes List

Boot mode	SOP3	SOP2	SOP1	SOP0
OSPI (4S) - Quad Read Mode	0	0	0	0
UART	0	0	0	1
OSPI (1S) - Single Read Mode	0	0	1	0
OSPI (8S) - Octal Read Mode	0	0	1	1

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Table 8-1. Boot Modes List (continued)

Boot mode	SOP3	SOP2	SOP1	SOP0
DevBoot	1	0	1	1
xSPI 8D (SFDP)	1	1	0	0
USB DFU	1	1	1	0
Unsupported boot mode	All other combinations are not defined			

8.4 LED Indicators

Each PHY provides two LED outputs (PHYx_LED1, PHYx_LED2) for link and activity indication. Connect LEDs through current-limiting resistors.

8.5 Thermal Considerations

The TICS100MOD is designed for operation up to +85°C ambient temperature. For optimal performance:

- Ensure adequate airflow in enclosed systems
- Avoid placing heat-generating components directly adjacent to the module
- Connect the exposed pad (EP) to the host ground plane for heat dissipation

8.6 PCB Layout Recommendations

General:

Keep high-speed differential traces away from switching power supplies.

Ethernet Differential Pairs:

- Route as 100Ω differential pairs, 50Ω single-ended for other signals
- Match trace lengths within each pair
- Avoid vias and stubs in differential pairs
- Maintain a solid return path (ground plane) beneath all MDI traces

EMI/EMC Considerations:

- Add TVS diodes like ESDS314DBVR on Ethernet ports for ESD protection
- Shielded Ethernet cables are recommended for noisy environments

8.7 Protocol Support Details

EtherCAT

Hardware-accelerated EtherCAT device functionality:

- Compliant with IEC 61158 Type 12
- Hardware processing for minimal latency
- Distributed clocks (DC) synchronization with SYNC0/1 and LATCH0/1 signals
- Minimum cycle time: 50µs

PROFINET

PROFINET IO Device functionality:

- Compliant with IEC 61158 Type 10
- RT (Real-Time) and IRT (Isochronous Real-Time) support
- Hardware-based frame processing
- LLDP for topology detection

EtherNet/IP

EtherNet/IP adapter implementation:

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- Compliant with ODVA specifications
- CIP (Common Industrial Protocol) support
- Implicit and explicit messaging

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

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TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *your package*), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *your device speed range*). Figure x provides a legend for reading the complete device name for any *your device* device.

For orderable part numbers of *your device* devices in the *your package* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *Silicon Errata*.

Figure 9-1. Device Nomenclature

9.1.1 Device Nomenclature Boilerplate

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

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9.2 Tools and Software

Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded

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applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Concise Description	Description

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

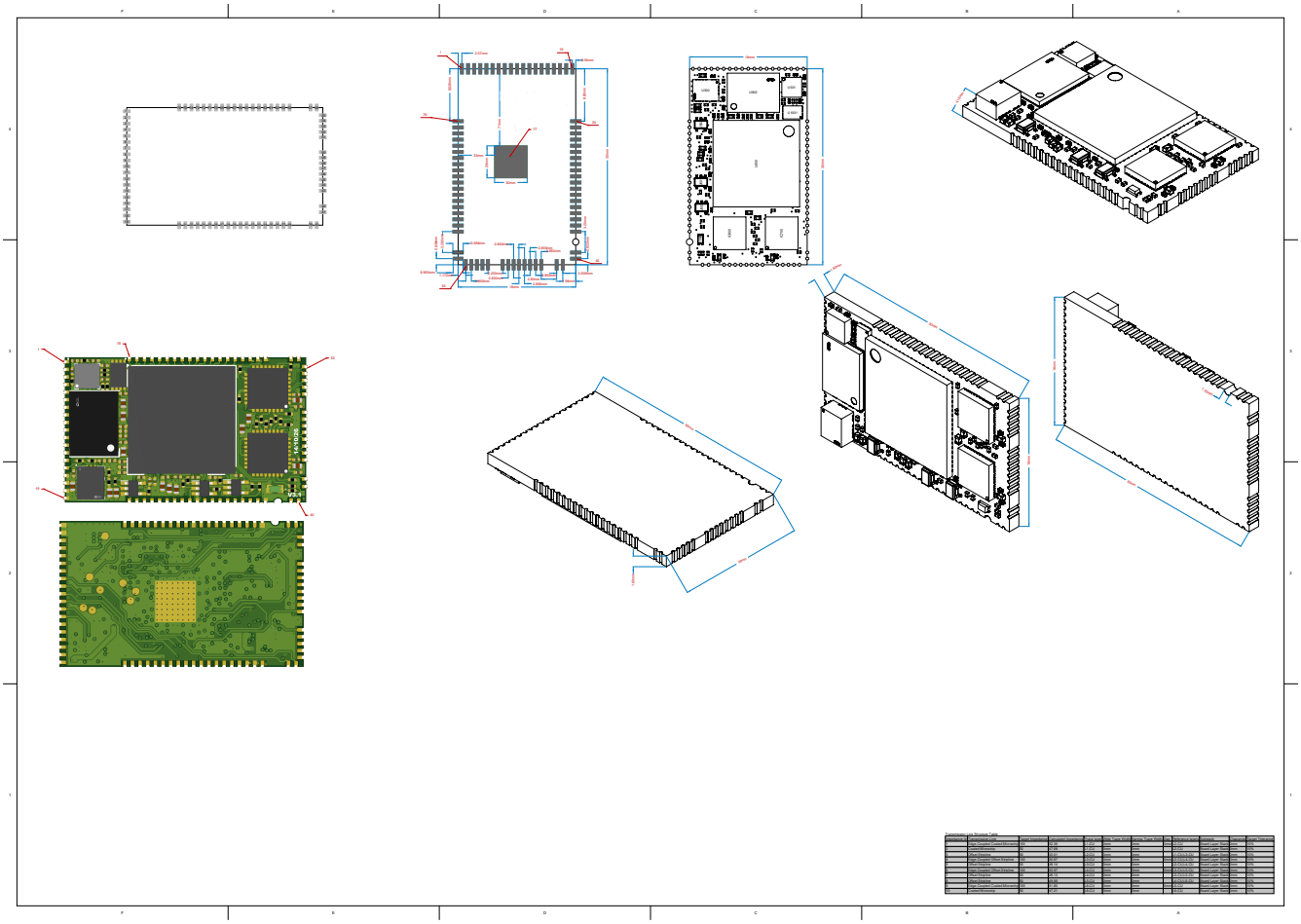
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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TICS100MODMUL	Preview	Production	null (null) | 0	1000 | NOT REQUIRED	-	Call TI	Call TI	-40 to 85	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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